UNIT - 4

* Bipolar Junction Transistor

→ Introduction
→ Txor construction
→ Txor operation
→ Txor current components
→ Txor as an amplifier
→ CB configuration
→ CE configuration
→ CC configuration
→ Limits of operation
→ Txor specifications

* Field Effect Transistor

→ JFET
→ Principle of operation
→ VI characteristics
→ Advantage of JFET over BJT
→ Introduction to MOSFETs
→ Depletion & Enhancement type MOSFETs
→ operation
→ VI characteristics.

(1)

J4, K2, M N2, N5, 6, 8, P3, 4 — (8)

Bipolar Junction Transistor

* Introduction

The transistor was invented by John Bardeen, Walter Brattain and William Shockley at Bell Laboratories in 1947.

A transistor is a semiconductor device, commonly used as an amplifier or an electrically controlled switch. Txor is a 3 terminal device :

i) Base ii) Emitter iii) Collector.

It can be operated in one of the three configurations :

i) Common base

ii) Common emitter

iii) Common collector

According to configuration, it can be used for voltage or current amplification.

TRANSISTOR = TRANSfer - resISTOR

The amplification in the transistor is achieved by passing input current signal from a region of low resistance to a region of high resistance. This concept of transfer of resistance has given the name TRANSfer - resISTOR. (TRANSISTOR).

There are two types of transistors :

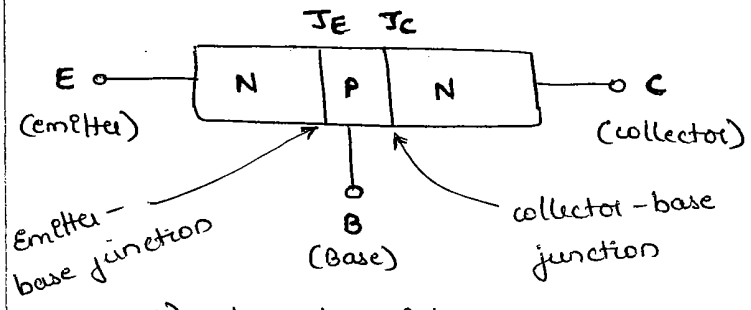
1. Unipolar Junction Transistor (UJT)
2. Bipolar Junction Transistor (BJT).

In unipolar junction txor, the current conduction is only due to one type of carriers i.e, majority charge carriers. The current conduction in bipolar junction txor is because of both the types of charge carriers i.e, holes and electrons. Hence it is called bipolar junction txor.

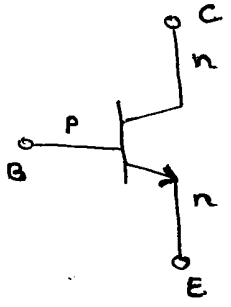
BJT is a semiconductor device in which one type of semiconductor is sandwitched between two opposite types of semiconductors. i.e, an n-type semiconductor is sandwitched between two p-type semiconductors (or) a p-type semiconductor

BJT are classified into two types:

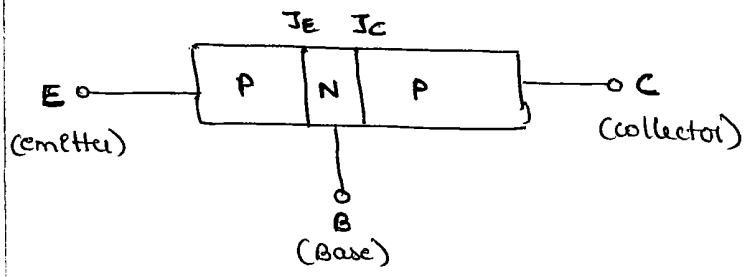
1. npn transistor.
2. pnp transistor.



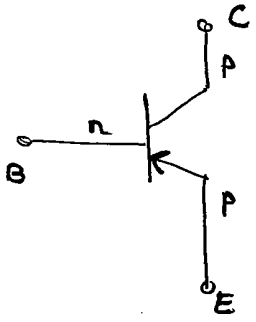
a) npn transistor.



Symbol.



b) pnp transistor



Symbol.

The arrow heads represents the conventional current direction from p to n.

The transistor has 3 teminals : Base, emitter and collector. It has 2 junctions :

i) Emitter-base junction (J_E)

ii) Collector-base junction (J_C)

Emitter: Emitter is **heavily doped** because it has to emit the charge carriers. (majority carriers).

Base: The charge carriers emitted by emitter should reach collector passing through the base as it is the middle region. Hence, base should be **very Thin** and to avoid recombination & to provide more collector current, base is **lightly doped.**

collector: Collector has to collect most of the charge carriers emitted by the emitter. Hence **area** of crossection of collector is **more** compared to emitter and it is **moderately doped.**

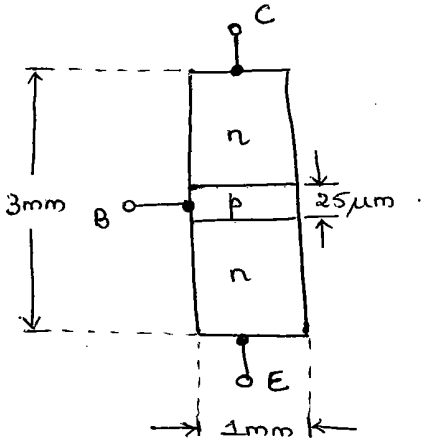
Five basic techniques have been developed for the manufacture of diodes, transistors and other semiconductor devices.

⇒ Such devices are classified into 5 types:

1. Grown Type
2. Alloy type
3. Electrochemically Etched type
4. Diffusion type
5. Epitaxial type.

a) Grown type:-

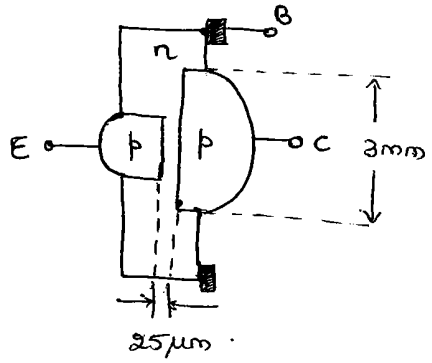
The npn grown-junction transistor is shown below



It is made of by drawing a single crystal from a melt of silicon or germanium whose impurity concentration is changed during the crystal operation by adding n and p-type atoms as required.

b) Alloy Type:-

This technique is ~~as~~ also called fused construction, and is shown below for an pnp transistor.



Here, the centre (base) section is a thin wafer of n-type material. Two small dots of Indium are attached to opposite sides of the wafer and the whole structure is raised for a short time to a high temperature, above the melting point of Indium but below that of germanium.

The Indium dissolves the germanium beneath it and forms a saturation solution. On cooling, the germanium in contact with the base material recrystallizes with enough Indium concentration to change it from n-type to p-type.

The collector is made larger than the emitter to withstand the heavy current & power dissipation at the collector base function.

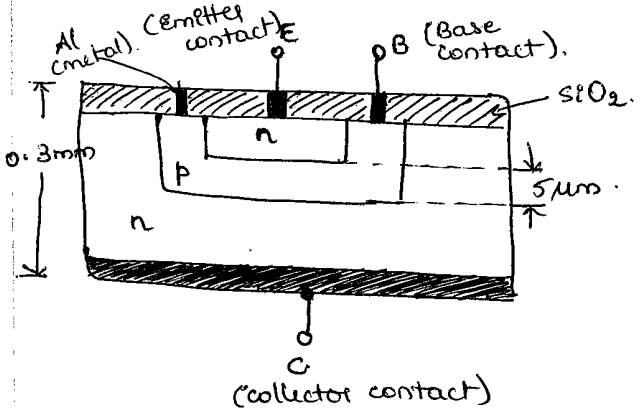
c) Electrochemically etched Type.

In this technique, etching depressions are made on opposite sides of a semiconductor wafer in order to reduce the thickness of the base region. The emitter & collector junctions are then formed by electroplating a suitable material into the depression areas.

This type of device, also referred to as surface-barrier transistor, is no longer of commercial importance.

d) Diffusion type:

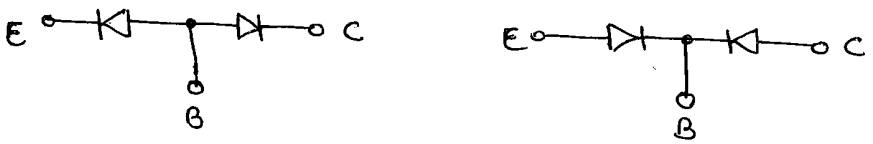
This technique consists of subjecting a semiconductor wafer to gaseous diffusions of both n and p type impurities to form both the emitter and collector junctions. A planar silicon transistor of diffusion type is shown below.



In this process, the base-collector junction area is determined by a diffusion mask which is photo etched just prior to the base diffusion.

The emitter is then diffused on the base, and a final layer of silicon dioxide (SiO_2) is thermally grown over the entire surface. Because of the passivating action of SiO_2, most surface problems are avoided & very low leakage currents result.

as shown below:



a) npn trot b) pnp trot.

However, we cannot replace a trot by two back-to-back diodes because

1. Relative doping levels in base, emitter and collector must be satisfied to act as a trot. Two normal p-n junction diodes cannot satisfy this requirement
2. In a trot, emitter-base junction is forward biased and collector-base junction is reverse biased. But due to diffusion process almost entire emitter current reaches to collector and base current is negligibly small. ⇒ due to diffusion device works as a trot, which cannot be achieved in a back-to-back diode configuration.
3. Emitter area is considerably smaller than collector area, because collector region has to handle more power than the emitter and more surface area is required for heat dissipation.

Transistor can be operated in 3 regions:

1. **Active Region**
2. **Saturation Region**
3. **Cut-off Region**

Active Region: J_E = forward biased, J_C = reverse biased.

Saturation Region: $J_E = J_C$ = forward biased.

Cut-off Region: $J_E = J_C$ = reverse biased.

In active region, trot acts as **amplifier**.

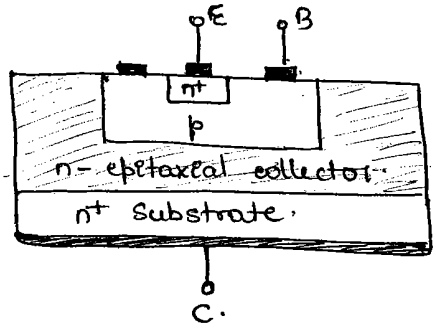
For a trot to operate as **switch**, it should be operated in saturation region for "ON" state and cut-off region for "OFF" state.

The most frequently employed method of manufacturing transistors today is the diffusion technique. This technique takes more time than the alloy process but it is relatively inexpensive and can be very accurately controlled.

The primary difference between diffusion & alloy process is the fact that liquification is not reached in diffusion process. Heat is applied only to increase the activity of elements involved in diffusion process.

c) Epitaxial type:-

The epitaxial technique consists in growing a very thin, high-purity, single-crystal layer of silicon or germanium on a heavily doped substrate of the same material. This augmented crystal forms the collector on which the base and emitter may be diffused. This type of transistor is shown below.

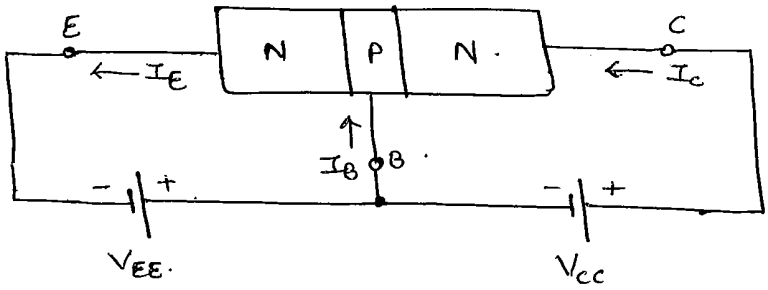


Epitaxial ⇒

"epi" means "upon"

"taxial" means "arrangement"

a) working of a npn transistor.



The npn transistor with base-to-emitter junction forward biased and collector to base junction reverse biased. is as shown above

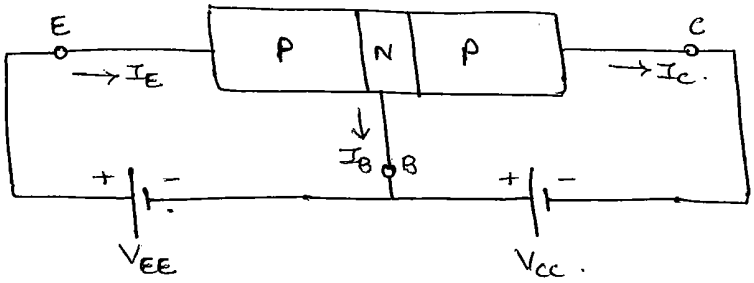
As the base to emitter junction is forward biased, the majority carriers emitted by the n-type emitter i.e electrons, have a tendency to flow towards the base which constitutes the emitter current, I_E.

As the base is p-type, there is a change of recombination of electrons emitted by the emitter with the holes in the p-type base. But as the base is very thin and lightly doped only few electrons emitted by the n-type emitter less than 5% combines with the holes in the p-type base, the remaining more than 95% electrons emitted by the n-type emitter cross-over into the collector region, constitute the collector current.

The current distribution as shown in the figure is.

$$I_E = I_B + I_C \longrightarrow (4.1)$$

a) working of pnp transistor.



The pnp transistor with base to emitter junction is forward biased and collector to base junction reverse biased is as shown above.

As the base to emitter junction is forward biased, The majority carriers emitter by the p-type emitter i.e holes, have a tendency to flow towards the base which constitutes the emitter current, I_E.

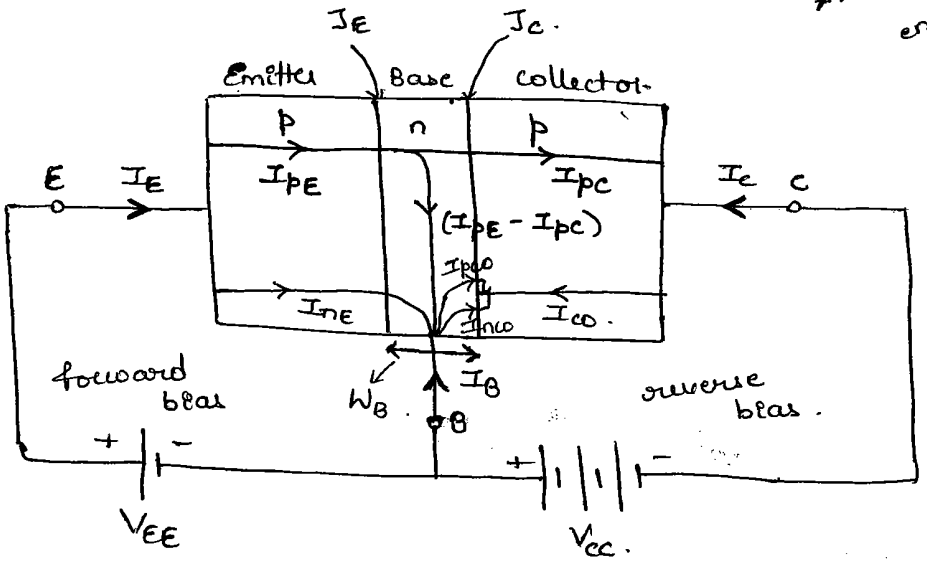
As the base is n-type, There is a chance of recombination of holes emitted by the emitter with the electrons in the n-type base. But as the base is very thin and lightly doped only few electrons less than 5% combine with the holes emitted by the p-type emitter, the remaining 95% charge carriers cross over the into the collector region to constitute the collector current

The current distributions are as shown

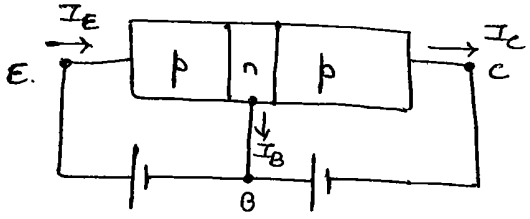
$$I_E = I_B + I_C.$$

The figure below shows the various current components which flow across the emitter junction (I_E) and collector junction (I_C) in a pnp trxor.

** consider all currents enter into trxor.



Here, a pnp transistor in common-base configuration is used. J_E is forward biased, J_C is reverse biased } ⇒ operated in active region

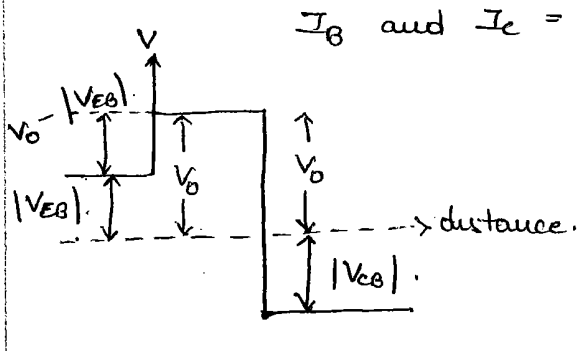


Since, J_E is forward biased I_E enters into transistor and I_B leaves the transistor.

Since, J_C is reverse biased. I_C leaves the trxor.

As, I_E, I_B and I_C are all considered entering into transistor, I_E = +ve and

I_B and I_C = −ve.



At J_E, since it is forward biased, potential barrier V_0 decreases by $|V_{EB}|$

At J_C, since it is reverse biased, potential barrier V_0 increases by $|V_{CB}|$.

Consider the forward biased emitter-base junction. Majority carriers holes of emitter diffuse into base producing a current I_{pE}. Illy, majority carriers electrons of base diffuse into emitter producing a current I_{nE}

Total emitter current is

$$\boxed{I_E = I_{pE} + I_{nE}.} \longrightarrow (4.2)$$

Since, Emitter is heavily doped and base is lightly doped, $I_{nE} << I_{pE} \Rightarrow \boxed{I_E \cong I_{pE}.} \longrightarrow (4.3)$

It is good to have $I_{nE} << I_{pE}$ because I_{nE} doesnot contribute the collector current.

The holes crossing the emitter base junction J_E and reaching the collector base junction J_C constitutes collector current I_{pC}, where

$$\boxed{I_{pC} = \alpha I_E.} \longrightarrow (4.4)$$

Not all the holes crossing the emitter junction J_E reach collector base junction J_C because some of them combine with the electrons of n-type base.

The possibility of recombination is very less due to following reasons

1. Base is lightly doped.
2. Diffusion constant of holes (L_p) is greater than width of base (W_B).

The recombination constitutes the base current. which is equal to $(I_{pE} - I_{pC})$ $\longrightarrow (4.5)$

Note:- currents entering into the terminal = positive

currents ~~entering~~ leaving into the terminal = negative

When emitter is open circuited,

$I_E = 0$ and hence $I_{pc} = 0$

Under this condition, the base and emitter collector together act as a reverse biased biased and I_c equals to reverse saturation current I_{co} (or I_{CBO}).

I_{co} = reverse saturation current at I_c

I_{CBO} = reverse saturation current at collector in common base with emitter open.

If surface leakage current due to impurities + current due to avalanche multiplication is considered then I_{CBO} is used else I_{co} is used.

I_{CBO} consists of two parts:

① I_{pco} caused by holes (minority carriers) moving across I_c from n-region to p-region

② I_{nco} caused by electrons (minority carriers) moving across I_c from p-region to n-region.

$$\Rightarrow \boxed{-I_{co} = -I_{CBO} = I_{pco} + I_{nco}} \longrightarrow (4.6)$$

If emitter is not open circuited i.e $I_E \neq 0$, Then

$$I_c = I_{CBO} - I_{pc} \longrightarrow (4.7)$$

$$\Rightarrow \boxed{I_c = -\alpha I_E + I_{CBO}} \longrightarrow (4.8)$$

[NOTE:- Collector current is sum of I_{pc} and I_{CBO} but not the difference]

Here, α = common base current gain

$$\boxed{\alpha = -\left(\frac{I_c - I_{CBO}}{I_E - 0}\right) = \frac{I_{pc}}{I_E}} \quad (\because I_c = I_{CBO} - I_{pc}) \longrightarrow (4.9)$$

Thus, "α" is defined as the ratio of change in collector current to change in emitter current as emitter junction bias is varied from open circuit to forward bias.

Neglecting, I_{CBO}, The common base dc current gain is given by

$$\alpha_{dc} = \frac{-I_c}{I_E} = \frac{I_{pc}}{I_E} \rightarrow (4.10)$$

The value of "α" will be nearly equal to "1". It generally varies from 0.95 to 0.995.

Generalized transistor equation that can be used for both forward & reverse bias at collector junction is

$$I_c = -\alpha I_E + I_{CBO}\left[1 - e^{V_{cc}/\eta V_T}\right] \rightarrow (4.11)$$

Emitter Injection efficiency or Emitter Efficiency (γ^*)

It is the ratio of current of injected carriers at emitter-base junction to total emitter current.

$$\gamma^* = \frac{\text{current of injected carriers at } I_E}{\text{total emitter current.}}$$

$$\gamma^* = \frac{I_{pE}}{I_{pE} + I_{nE}} = \frac{I_{pE}}{I_E} \rightarrow (4.12)$$

since, emitter is heavily doped, $I_{pE} >> I_{nE} \Rightarrow \gamma^* \simeq 1$

Transport factor or Base transport factor (β^*)

It is the ratio of injected carrier current reaching at collector base junction I_C to injected carrier current at emitter base junction I_E.

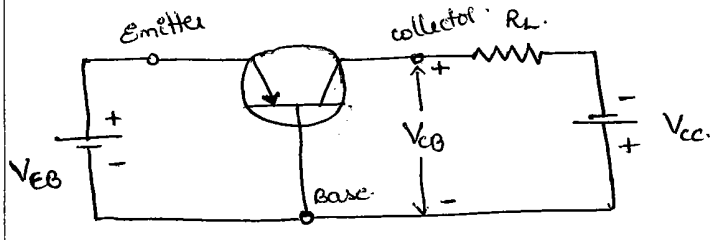
$$\beta^* = \frac{\text{current transported to collector.}}{\text{total current injected into base at } I_E.}$$

$$\beta^* = \frac{I_{pc}}{I_{pE}} \rightarrow (4.13)$$

Relation between α, β^*, γ^*

$$\alpha = \frac{I_{pc}}{I} = \frac{I_{pc}}{I_{pE}} \times \frac{I_{pE}}{I} = \beta^* \cdot \gamma^* = \alpha \rightarrow (4.14)$$

A load resistor R_L is in series with the collector supply voltage V_{cc} as shown below.



As small voltage change ΔV_i between emitter & base causes a relatively large emitter current ΔI_E.

That fraction of ~~this~~ current change which is collected & passes through R_L is defined by the symbol α'.

change in output voltage across load resistor, R_L } $= \boxed{\Delta V_o = \alpha' . R_L . \Delta I_E} \rightarrow (4.15)$

= many times the change in input voltage, ΔV_i

Under these circumstances, the voltage amplification,

$\boxed{A = \dfrac{\Delta V_o}{\Delta V_i}}$ will be greater than Unity. $\rightarrow (4.16)$

$\Rightarrow$ transistor acts as amplifier

If the dynamic resistance of emitter junction is r_e'

Then

$$\Delta V_i = r_e' . \Delta I_E \rightarrow (4.17)$$

and $$A = \frac{\alpha' . R_L . \Delta I_E}{r_e' . \Delta I_E .} = \boxed{\frac{\alpha' . R_L}{r_e'} = A} \rightarrow (4.18)$$

where $\boxed{r_e' = \dfrac{26}{I_E}} \rightarrow (4.19)$

Eg:- $r_e' = 40\,\Omega$, $\alpha' = -1$ and $R_L = 3000\,\Omega$.

Then $A = -75$.

This calculation is over simplified, but in essence it is correct and gives a physical explanation of why transistor

The transistor provides power gain as well as voltage & current gain. So it is clear that current in the low resistance i/p circuit is transferred to the high resistance output circuit.

The parameter α'

The parameter α' is defined as the ratio of the change in the collector current to the change in the emitter current at constant collector to base voltage and is called the small signal forward short circuit current transfer ratio or gain.

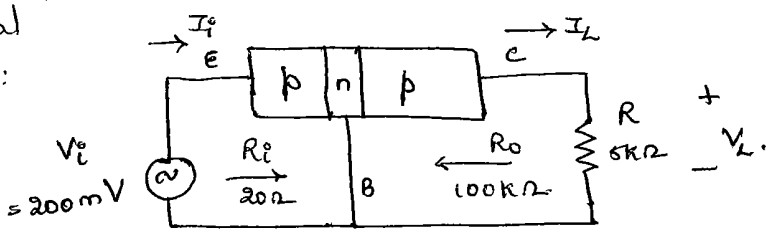
$$\alpha' = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB} = \text{constant}} \rightarrow (4.20)$$

On the assumption that α' is independent of I_E,

Then from the eq $I_c = -\alpha I_E + I_{CBO}$.

$$\alpha' = -\alpha. \rightarrow (4.21)$$

Numerical Example :



$$I_i = \frac{V_i}{R_i} = \frac{200mV}{20\Omega} = 10mA.$$

If we assume $\alpha = 1$

$$I_E = I_c \Rightarrow I_i = I_L = 10mA.$$

$$\Rightarrow V_L = I_L \cdot R = 10 \times 10^{-3} \times 5 \times 10^3$$
$$= 50V.$$

Voltage amplification, $A_V = \frac{V_o}{V_i} = \frac{50V}{200mV} = 250$.

Since $\alpha \leq 1$ & $I_c = \alpha I_E$ current amplification $\frac{I_c}{I_E} < 1$

Typical values

$R_i \rightarrow 10\Omega$ to 100Ω

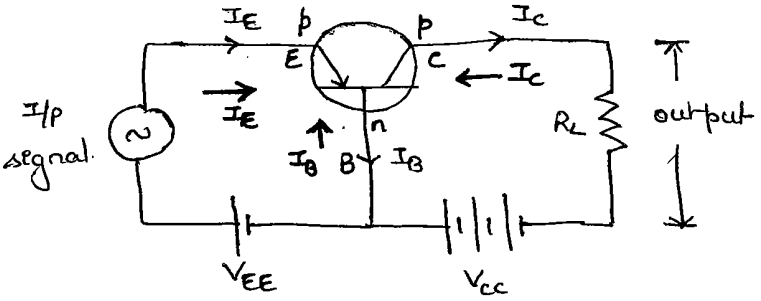
$R_L \rightarrow 50K\Omega$ to $100M\Omega$

$A_V \rightarrow 50$ to 300

In this configuration, the i/p signal is applied between emitter and base while the o/p is taken from collector & base. As base is common to i/p and o/p circuit, this configuration is called common-base configuration

*** Assume, all currents enter into trxr

a) pnp trxr

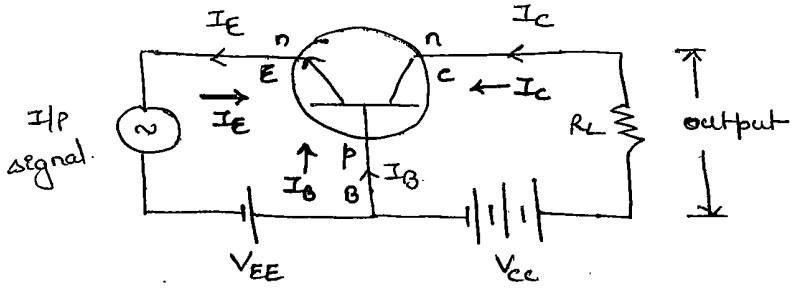


$I_E = I_C + I_B$

$\alpha_{dc} = \frac{-I_C}{I_E}$

(I_C & I_E are opposite i.e I_C flows out of trxr & I_E flows into trxr)

b) npn trxr



$I_E = I_C + I_B$.

$\alpha_{dc} = \frac{-I_C}{I_E}$.

(I_C & I_E are opposite i.e I_C flows into trxr, & I_E flows out of trxr).

When no signal is applied, then the ratio of the collector current to the emitter current is called **dc alpha (α_{dc})** of a trxr (or) **current amplification factor**.

$$\alpha_{dc} = \frac{-I_C}{I_E} \longrightarrow (4.22)$$

Note:- -ve sign signifies that I_E flows into trxr and I_C flows out of it for pnp trxr. and reverse for npn trxr.

α of a trxr is a measure of the quality of a trxr. higher is the value of α, better is the trxr in the sense that collector current approaches the emitter current.

$$I_C = \alpha_{dc} I_E$$

and $I_B = I_E - I_C$.

$$\Rightarrow I_B = I_E - \alpha_{dc} I_E$$

$$\Rightarrow \boxed{I_B = (1-\alpha_{dc}) I_E.} \longrightarrow (4.23)$$

When signal is applied, the ratio of change in the collector current to the change in emitter current at constant collector-base voltage is defined as **current amplification factor**.

$$\boxed{\alpha_{ac} = -\frac{\Delta I_C}{\Delta I_E}.} \longrightarrow (4.24)$$

For all practical purposes, $\alpha_{dc} = \alpha_{ac} = \alpha$ and practical values in commercial trans range from 0.9 to 0.99.

The **total collector current** consists of two parts:

a) αI_E, current due to majority carriers

b) I_{CBO}, current due to minority carriers.

$\Rightarrow$ total collector current

$$I_C = -\alpha I_E + I_{CBO}$$
(majority) (minority)

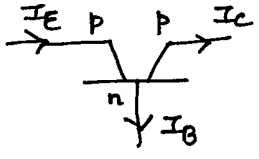
but $I_E + I_B + I_C = 0$ (∵ assumed that all currents enter into trans).

$$\Rightarrow I_C = \alpha (I_B + I_C) + I_{CBO}.$$

$$I_C (1-\alpha) = \alpha I_B + I_{CBO}$$

$$\boxed{I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO}} \longrightarrow (4.25)$$

Note:- If original directions are assumed.



Then $\alpha = \frac{I_C}{I_E}$ and $I_E = I_B + I_C$

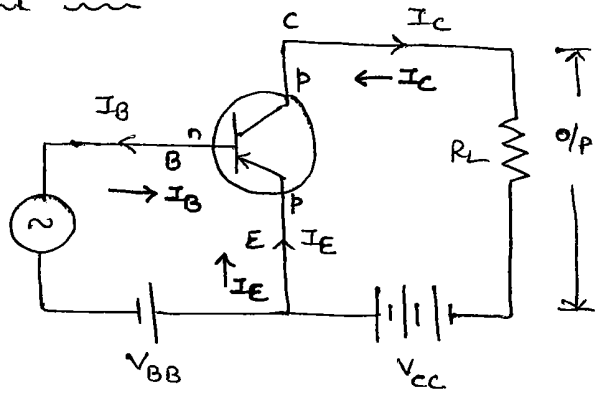
and $I_C = \alpha I_E + I_{CBO}$

Considering only magnitudes. $\Rightarrow I_C = \alpha (I_B + I_C) + I_{CBO}$

$\boxed{I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO}}$ (4.25)

In this configuration, the i/p signal is applied between base and emitter and the o/p is taken from collector & emitter. As emitter is common to i/p and o/p circuits, hence the name common-emitter configuration.

a) pnp txtr.

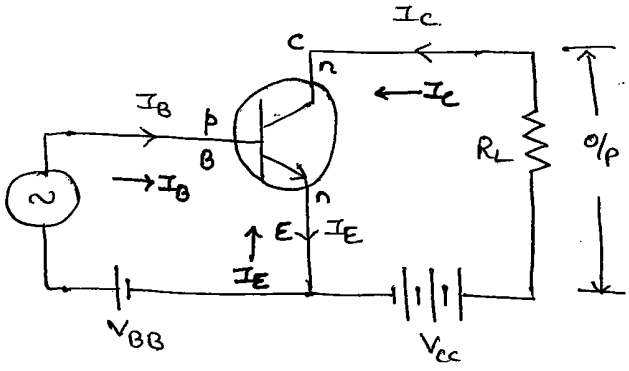


$$I_E = I_B + I_C$$

$$\beta = \frac{I_C}{I_B}$$

(Both I_C & I_B go o/p of txtr $\Rightarrow$ β = +ve)

b) npn txtr



$$I_E = I_B + I_C$$

$$\beta = \frac{I_C}{I_B}$$

(Both I_C & I_B go into the txtr $\Rightarrow$ β = -ve)

When no signal is applied, Then the ratio of collector current to the base current is called **dc beta** (β_{dc}) of a txtr.

$$\beta_{dc} = \beta = \frac{I_C}{I_B}. \quad \longrightarrow (4.26)$$

When signal is applied, the ratio of change in collector current to the change in base current is defined as **base current amplification factor**.

$$\beta_{ac} = \beta = \frac{\Delta I_C}{\Delta I_B}. \quad \longrightarrow (4.27)$$

$$\Rightarrow I_C = \beta I_B \quad \longrightarrow (4.28)$$

Almost all the TRUSS, the base current is less than 5%
of the emitter current. Due this fact, β is generally greater than 20. Usually, β ranges from 20 to 500.

⇒ This configuration is frequently used when appreciable current gain as well as voltage gain is required.

The **total collector current**,

$$I_C = \beta I_B + I_{CEO} \longrightarrow (4.29)$$

where I_{CEO} = leakage current.

But, we have $I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$.

comparing eq (4.25) and (4.29) we get.

$$\boxed{\beta = \frac{\alpha}{1-\alpha}} \text{ and } \boxed{I_{CEO} = \frac{1}{1-\alpha} I_{CBO}} \longrightarrow (4.30)$$

Relation between α and β:

We know that $\alpha = \frac{I_C}{I_E}$ and $\beta = \frac{I_C}{I_B}$.

and $I_E = I_B + I_C \Rightarrow I_B = I_E - I_C$.

$$\Rightarrow \beta = \frac{I_C}{I_E - I_C}$$

$$= \frac{I_C/I_E}{1 - I_C/I_E} = \frac{\alpha}{1-\alpha}.$$

$$\Rightarrow \boxed{\beta = \frac{\alpha}{1-\alpha}} \longrightarrow (4.31)$$

$$\beta(1-\alpha) = \alpha.$$

$$\Rightarrow \beta - \alpha\beta = \alpha. \Rightarrow \alpha(1+\beta) = \beta.$$

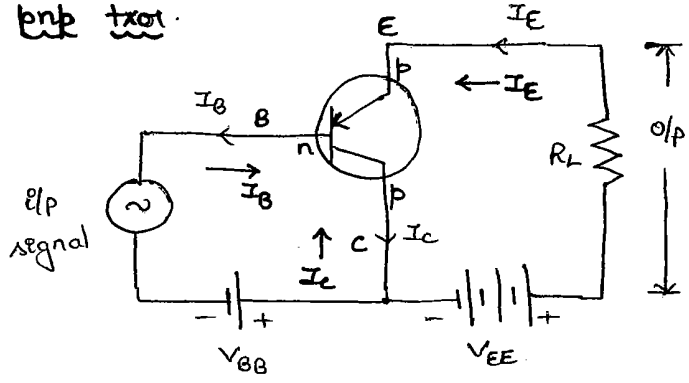
$$\Rightarrow \boxed{\alpha = \frac{\beta}{1+\beta}} \longrightarrow (4.32)$$

It can be also seen that $\boxed{1-\alpha = \frac{1}{1+\beta}} \longrightarrow (4.33)$

$$\Rightarrow \boxed{I_C = \beta I_B + (1+\beta) I_{CBO}} \longrightarrow (4.34)$$

In this configuration, the i/p signal is applied between base and collector and the o/p is taken from the emitter. As, collector is common to i/p and o/p circuits, hence the name common collector configuration.

a) pnp txor.

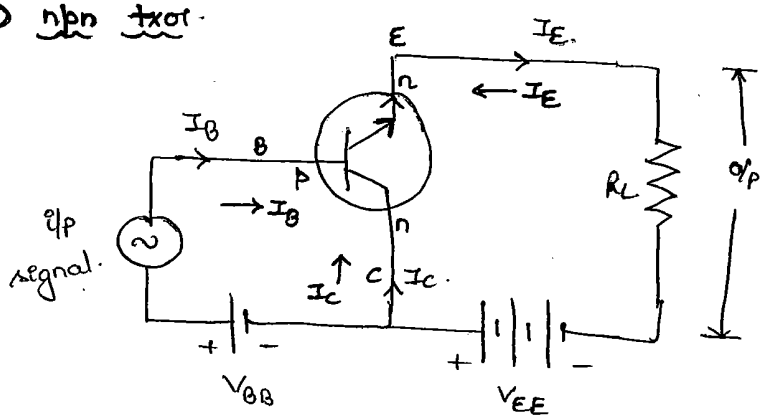


$I_E = I_B + I_C$

$\gamma = \frac{-I_E}{I_B}$

($\because$ I_E & I_B are opposite i.e, I_E enters into txor, I_B leaves the txor).

b) npn txor.



$I_E = I_B + I_C$

$\gamma = \frac{-I_E}{I_B}$

($\because$ I_E & I_B are opposite i.e I_E leaves txor, I_B enters into txor)

when no signal is applied, then the ratio of emitter current to the base current is called as **dc gamma (γ_{dc})** of a txor.

$$\gamma_{dc} = \gamma = \frac{-I_E}{I_B} \quad \rightarrow (4.36)$$

-ve sign indicates that I_E flows into txor & I_B flows out of the txor for pnp and reverse in npn.

when signal is applied, then the ratio of change in emitter current to the change in base current is known as **current amplification factor, γ.**

$$\gamma_{ac} = \gamma = \frac{-\Delta I_E}{\Delta I_B} \quad \rightarrow (4.37)$$

This configuration provides the same current gain as common emitter circuit as $\Delta I_E \approx \Delta I_C$, but voltage gain is less than 1.

We know that, $I_E = I_B + I_C$.

~~All currents are assumed entering into the node.~~

Also, $I_C = +\alpha I_E + I_{CBO}$

considering only magnitudes.

$\Rightarrow$ $I_E = I_B + \alpha I_E + I_{CBO}$

$$I_E = \frac{I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}.$$

(or) $\boxed{I_E = (1+\beta) I_B + (1+\beta) I_{CBO}}$ → (4.38) $\left(\because \frac{1}{1-\alpha} = 1+\beta\right)$.

This is the total emitter current.

Relation between γ and α.

we know that, $\gamma = \frac{I_E}{I_B}$ (considering only magnitudes)

and $\alpha = \frac{I_C}{I_E}$

Also, $I_B = I_E - I_C$.

Now, $\gamma = \frac{I_E}{I_E - I_C} = \frac{1}{1 - \frac{I_C}{I_E}} = \frac{1}{1-\alpha}$.

$\Rightarrow$ $\boxed{\gamma = \frac{1}{1-\alpha}}$ → (4.39)

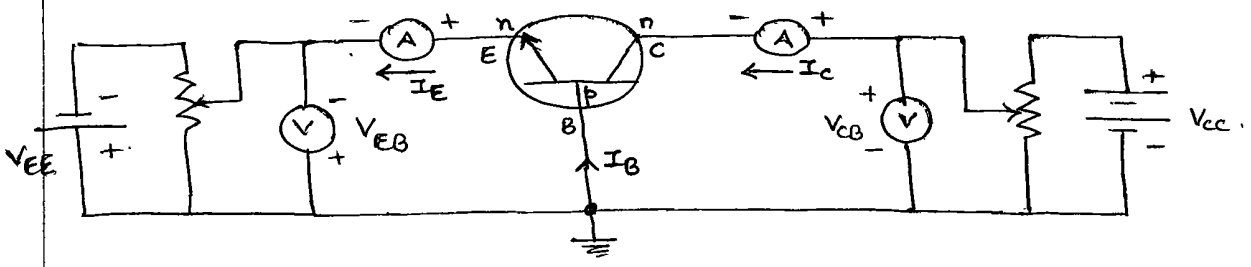
Relation between γ and β.

We know that $\frac{1}{1-\alpha} = 1+\beta$.

$\Rightarrow$ $\boxed{\gamma = 1+\beta}$ → (4.40)

$\Rightarrow$ $\boxed{\gamma = \frac{1}{1-\alpha} = 1+\beta}$

The circuit diagram for determining the characteristics of npn transistor in CB configuration is shown below:



We can completely describe the transistor with the following two relations,

$$V_{EB} = \phi_1 (V_{CB}, I_E)$$

$$I_E = \phi_2 (V_{CB}, I_E).$$

V_{CB}, I_E → Independent parameters

V_{EB}, I_C → variables dependent on V_{CB}, I_E

The plot between emitter-base voltage V_{EB} and emitter current I_E, with collector-to-base voltage V_{CB} as a parameter is a set of curves referred to as **input or emitter, static characteristics**.

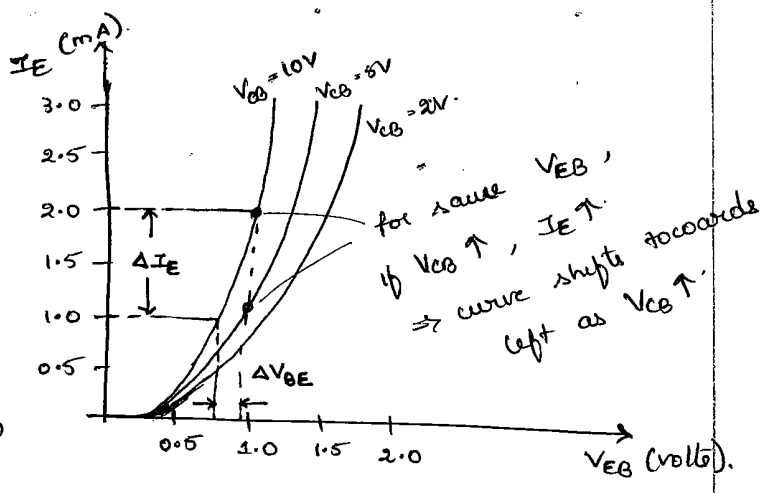
The plot between collector current I_C and collector-to-base voltage V_{CB}, with emitter current I_E as a parameter is a set of curves referred to as **output or collector, static characteristics**.

a) Input characteristics

To determine the i/p characteristics, use the relation

$$V_{EB} = \phi_1 (V_{CB}, I_E)$$

Here, V_{CB} is kept constant and I_E is increased from 0 in suitable equal steps by increasing V_{EB}. This is repeated for higher fixed values of V_{CB}. A curve is drawn between emitter current I_E and emitter-base voltage V_{EB} at constant collector-base voltage V_{CB}.



1. After cut-in voltage (barrier potential, normally 0.7V for silicon and 0.3V for germanium), the emitter current (I_E) increases rapidly with small increase in emitter-base voltage (V_{EB}).

⇒ I/p resistance is very small.

∴ Since, I/p resistance is a ratio of change in emitter-base voltage (ΔV_{EB}) to the resulting change in emitter current (ΔI_E), at constant collector-base voltage (V_{CB}), this resistance is also known as the dynamic I/p resistance of the txor in CB configuration.

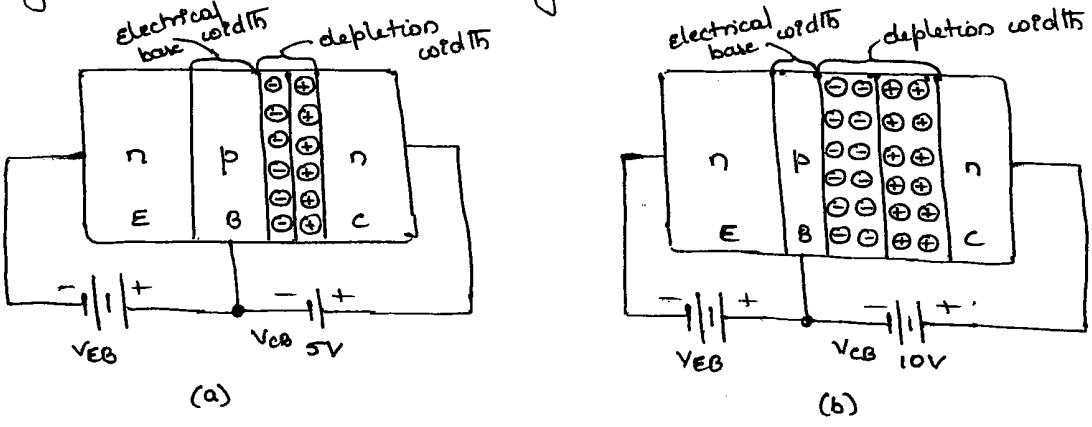
$$r_i = \left.\frac{\Delta V_{EB}}{\Delta I_E}\right|_{V_{CB} = \text{constant}}$$

2. An increase in magnitude of collector voltage will, by Early effect, cause the emitter current to increase, with V_{EB} held constant.

⇒ curve shifts towards left as $|V_{CB}|$ increases.

Early Effect :-

The change in base and depletion region width with change in reverse biased voltage is shown below:



When the reverse bias voltage V_{CB} increases, the width of the depletion region also increases, which reduces the electrical base width. This effect is called "Early Effect" or "Base width modulation".

Due to reduction of electrical base width, concentration of the charge gradient increases in the base region. This causes more diffusion of electrons from n-type emitter to p-type base increasing I_E slightly.

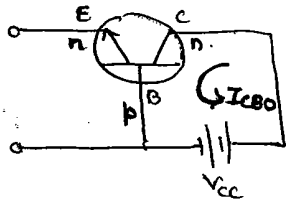
1. There is less chance of recombination within the base region. Hence, transport factor β^* and also α, increase with this an increase in the magnitude of collector junction voltage.
2. Charge gradient is increased within the base, and consequently, the current of minority carriers injected across the emitter junction increases.

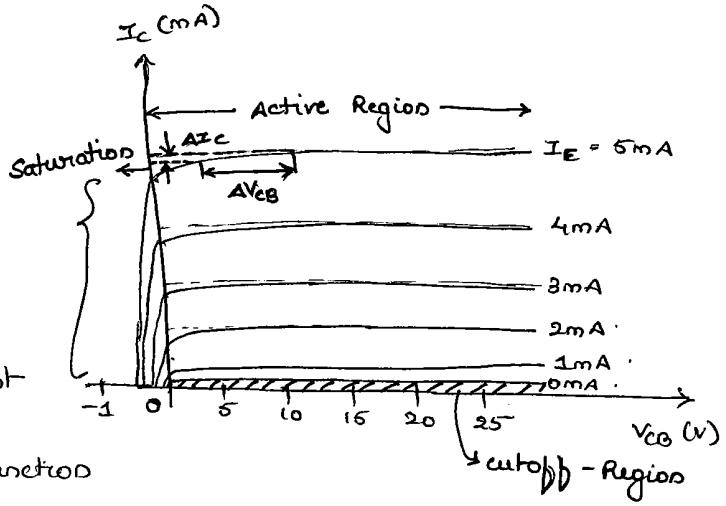
b) **Output characteristics**

The collector-base junction is normally reverse-biased.

⇒ If $I_E = 0$, the collector current $I_c = I_{CBO} = I_{CO}$.

where I_{CBO} = leakage current
- → emitter open
- → collector base junction





Note :- I_{CO} is +ve for npn txor
I_{CO} is −ve for pnp txor.

$I_C = \phi_2 (V_{CB}, I_E)$
↳ constant.

c) **Active Region** — Amplifier

In this region, collector junction is reverse biased and emitter junction is forward biased.

If $I_E = 0$, then I_c is small & equals to I_{CO} (μA for Ge and nA for Si).

Suppose that a forward emitter current I_E flows in the emitter circuit, then a fraction $-\alpha I_E$ of this current will reach the collector and I_E is given

$$I_C = -\alpha I_E + I_{CO}$$ (for npn txor, I_{CO} = +ve
for pnp txor, I_{CO} = −ve).

In active region, the collector current is essentially independent of collector voltage and depends upon the emitter current. However, because of early effect, actually there is a small increase in $|I_c|$ with $|V_{CB}|$. ⇒ $r_o = \left.\frac{\Delta V_{CB}}{\Delta I_C}\right|_{I_E = \text{constant}}$ = very high

Because α is less than, but almost equal to, unity, the magnitude of the collector current is slightly less than that of emitter current.

ii) **Saturation Region** — ON switch

The region to the left of the ordinate, $V_{CB} = 0$ and above the $I_E = 0$ characteristics, in which both emitter & collector junctions are forward biased, is called the saturation region.

Actually, V_{CB} is slightly negative for npn trxr in this region (+ve for pnp trxr) and this forward biasing of the collector current accounts for large change in I_C with small changes in V_{CB}.

iii) **Cut-off Region** — OFF switch

The region below and to the right of the $I_E = 0$ characteristic, for which the emitter and collector junctions are both reverse biased, is referred to as cutoff region. here $I_C = I_{CBO}$

To determine the o/p characteristics, use the relation

$$I_C = \phi_2 \ (V_{CB}, I_E)$$

Here, emitter current I_E is kept constant at a suitable value by adjusting the emitter-base voltage V_{EB}. Then V_{CB} is increased in suitable equal steps and the collector current I_C is noted for each value of I_E.

This is repeated for different fixed values of I_E. Now, the curves of I_C verses V_{CB} are plotted for constant values of I_E and the o/p characteristics thus obtained is shown above.

* Transistor Parameters

i) I/p Impedance, $h_{ib} = \left.\frac{\Delta V_{EB}}{\Delta I_E}\right|_{V_{CB} = \text{constant}}$, 20 to 50 Ω

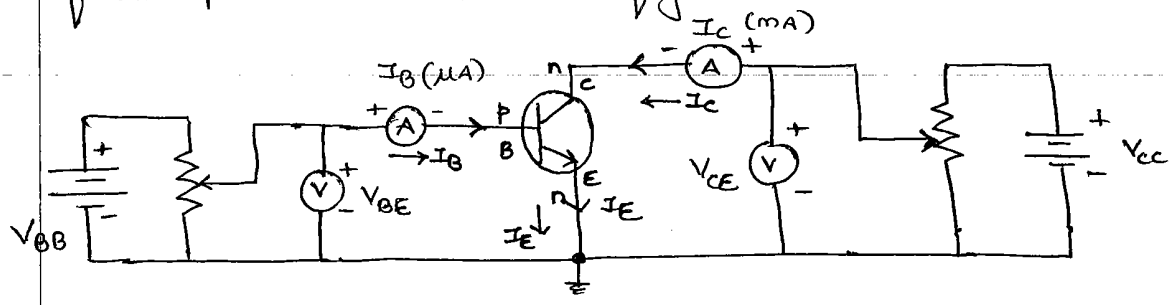
ii) o/p Admittance, $h_{ob} = \left.\frac{\Delta I_C}{\Delta V_{CB}}\right|_{I_E = \text{constant}}$, 0.1 to 10 μmhos.

iii) Forward current gain, $h_{fb} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB} = \text{constant}}$, 0.9 to 1.0

iv) Reverse voltage gain, $h_{rb} = \left.\frac{\Delta V_{EB}}{\Delta V_{CB}}\right|_{I_E = \text{constant}}$, 10^{-5} to 10^{-4}

Static characteristics of CE configuration

The circuit diagram for determining the static characteristics of an npn trxor in the CE configuration is shown below:



We can completely describe the trxor with the following 2 relations:

$$V_{BE} = f_1 (V_{CE}, I_B)$$

$$I_C = f_2 (V_{CE}, I_B)$$

The plot between ~~emitter~~ base-emitter voltage (V_{BE}) and base current (I_B), with collector-to-emitter voltage (V_{CE}) as a parameter, is a set of curves referred to as i/p, or base, characteristics.

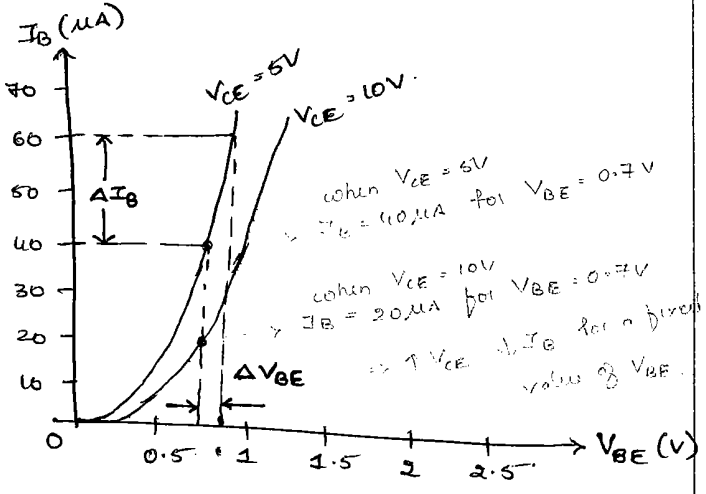
The plot between collector current (I_C) and collector-to-emitter voltage (V_{CE}), with base current (I_B) as a parameter, is a set of curves referred to as o/p or collector characteristics.

a) Input characteristics

To determine the i/p characteristics, use the relation

$$V_{BE} = f_1 (V_{CE}, I_B)$$

Here, V_{CE} is kept constant at zero volt and base current I_B is increased from 0 in steps by increasing V_{BE} in the circuit. The value of V_{BE} is noted for each setting of I_B



This procedure is repeated for higher fixed values of V_{CE} and the curves of I_B Vs V_{BE} are drawn.

From the characteristic curves we observe

1. With the collector shorted to emitter ($V_{CE} = 0$), the i/p characteristic is same as that of a forward biased diode. ⇒ i/p characteristic resemble a family of forward biased diode curves.

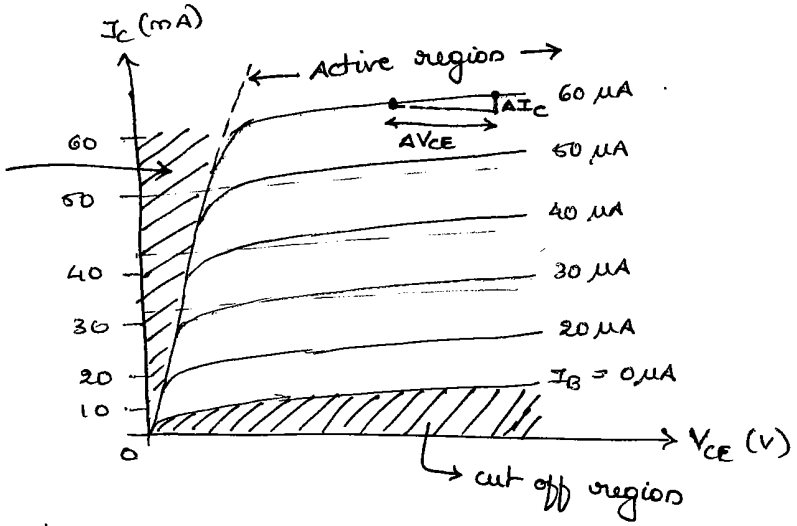
2. After cutin voltage the base current (I_B) increases rapidly with a small increase in base ~~current~~ emitter voltage (V_{BE}). ⇒ dynamic i/p resistance in CE is very small.

$$r_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$$

3. A larger value of V_{CE} results in a large reverse bias at collector-base pn junction. This increases the depletion region and reduces the effective width of the base. (Early effect).
⇒ There are fewer recombinations in the base region, reducing the base current I_B.

Thus, for a fixed value of V_{BE}, I_B decreases as V_{CE} is increased ⇒ As $|V_{CE}|$↑ curves shift towards right.

b) Output characteristics



To determine the o/p characteristics, use the relation,

$$I_C = f_2(V_{CE}, I_B)$$

Here, I_B is kept constant at a suitable value by adjusting base-emitter voltage, V_{BE}. The magnitude of V_{CE} is increased suitably in equal steps from zero and the collector current I_C is noted for each setting of V_{CE}.

Now, the curves of I_C Vs V_{CE} for different constant values of I_B are plotted.

o/p dynamic resistance, $r_o = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B = \text{constant (or) } \Delta I_B = 0}$

This is high in CE

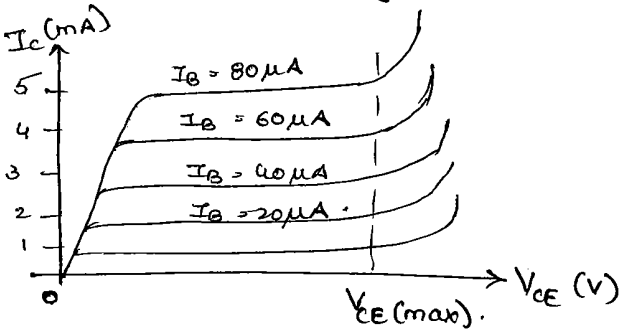
Active region:

The region where the curves are approximately horizontal is the active region of the CE configuration. Here, I_C is Reverse biased.

As V_{CE} is increased, reverse bias increases. This causes depletion region to spread more in base than in collector, reducing the chances of recombinations in the base $\Rightarrow \alpha_{dc} \uparrow$.

This early effect causes collector to rise more sharply with increasing V_{CE} in the active region of o/p characteristics of CE. For the same reason, CE o/p characteristics are sloping upwards, when compared to CB o/p characteristics.

In active region, the collector junction is R.B. For every transistor there is limit on the maximum value for this reverse bias voltage. If this limit is exceeded, breakdown occurs in trxor This effect is commonly known as **punch through effect**.



This large current may damage the trxor.

If $V_{CB} \uparrow$, depletion region $\uparrow$. At large values of V_{CB}, base is completely full of depletion region & hence no recombination can take place in base and hence the relationship $I_C = \beta I_B$ is not retained $\Rightarrow$ transistor action is lost & breakdown occurs.

Cutoff Region:

$$I_C = \beta I_B + I_{CEO}$$

when $I_B = 0$, I_C = reverse saturation current, I_{CEO}

Inorder to bring trxor into cutoff, $I_B = 0$ and I_E should be R.B i.e cutoff as defined as the condition where collector current is equal to reverse saturation current with emitter current, $I_E = 0$.

Saturation Region

$I_E = I_C$ = F.B, with $V_{CE(sat)} = 0.1$ to 0.3 V.

O/p current

Why CE is widely used in amplifier circuit?

→ CE is the only configuration which provides both current & voltage gain greater than unity.

Power gain = voltage gain × current gain

This is maximum for CE

→ In CE ratio of o/p to i/p resistance is small, may be in the range from 10 to 100 ⇒ ideal for coupling b/w various stages of transistors.

Maximum power is transferred from stage 1 to stage 2, if o/p resistance of stage 1 is equal to i/p resistance of stage 2.

* Transistor parameters.

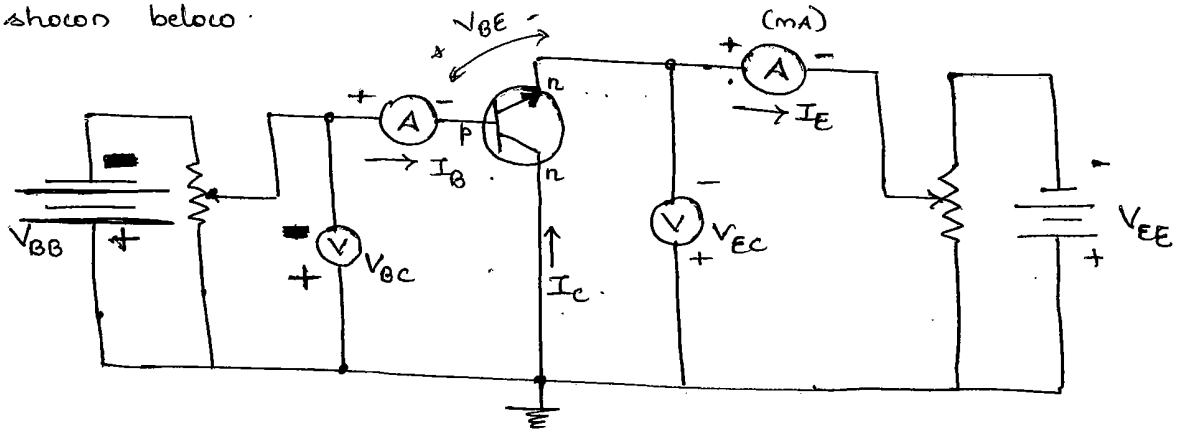
i) Input impedance, $h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$, 500 to 2000 Ω

ii) output admittance, $h_{oe} = \left.\frac{\Delta I_C}{\Delta V_{CE}}\right|_{I_B = \text{constant}}$, 0.1 to 10 μmhos

iii) Forward current gain, $h_{fe} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$, 20 to 200

iv) Reverse voltage gain, $h_{re} = \left.\frac{\Delta V_{BE}}{\Delta V_{CE}}\right|_{I_B = \text{constant}}$, 10^{-5} to 10^{-4}

The circuit diagram for determining the static characteristics of an npn transistor in the common collector configuration is shown below.



we can completely describe the transistor with the following two relations,

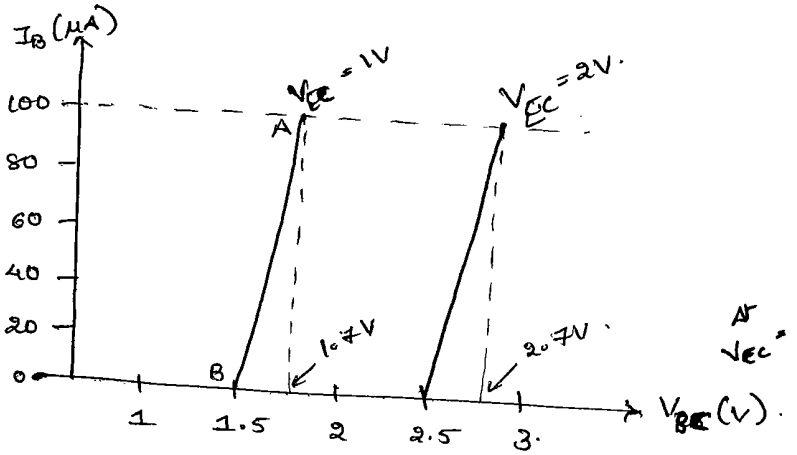
$$V_{BC} = \psi_1 (V_{EC}, I_B).$$

$$I_E = \psi_2 (V_{EC}, I_B).$$

The plot between base-collector voltage (V_{BC}) and base current (I_B), with emitter-to-collector voltage (V_{EC}) as a parameter, is a set of curves referred to as I/p characteristics.

The plot between emitter current (I_E) and emitter-to-collector voltage (V_{EC}), with base current as a parameter, is a set of curves referred to as o/p characteristics.

a) Input characteristics.



$V_{EC} = V_{EB} + V_{BC}$.

$= V_{BC} - V_{BE}$

here,

V_{BC} is largely dependent on V_{EC}.

$V_{EC} = V_{BC} - V_{BE}$.

At $V_{EC} = 1V$ $\Rightarrow V_{BE} = V_{BC} - V_{EC}$.

$= 1.7 - 1$.

$= 0.7V$.

As long as, $V_{BE} > V_\gamma$, I_E = F.B

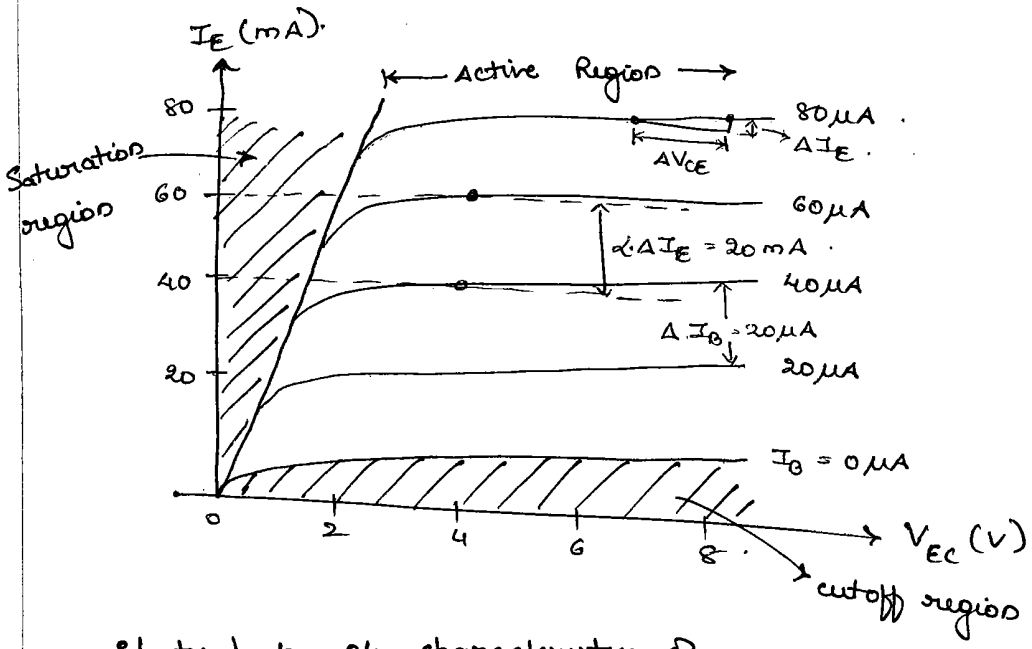
∴ forward (from figure).

If $V_{EC} = 1V$ while V_{BC} is increased to 1.0V (point B).

then at point B, $V_{BE} = 1.5 - 1 = 0.5V$.

⇒ as V_{BE} is reduced from 0.7 to 0.5V, current has reduced from 100μA to 0μA ($\because$ 0.5V is not sufficient to FB).

b) Output characteristics



Identical to o/p characteristics of CE configuration except that the slope of curve is more in CC.

* Typical NPN transistor junction voltages at 25°C

	V_{BE} (cutoff)	V_γ (or) V_{BE} (cutin)	V_{BE} (active) or V_{BE} (ON)	V_{BE} (sat)	V_{CE} (sat)
Ge	0.1 V	0.1V	0.2V	0.3V	0.1V
Si	0.0V	0.5V	0.7V	0.8V	0.2V.

Note :- For PNP transistor all the above voltages have opposite polarity with same magnitude.

A Comparison of CB, CE and CC

Property	CB	CE	CC
. Input resistance	Low (about 100 Ω)	Moderate (~ 750 Ω)	High (about 750KΩ)
o/p resistance	High (about 450 KΩ)	Moderate (~ 45KΩ)	Low (about 25 Ω)
. current gain	1	High	High
. voltage gain	About 150	About 500	Less Than 1
. Phase shift b/w i/p & o/p voltages	0 or 360°	180°	0 or 360°
. Applications	for high frequency circuits	for audio frequency circuits	for impedance matching
	$\alpha = 0.98$ (current gain)	$\beta = 49$ (current gain)	$\gamma = 50$ (current gain).

has $I_{CBO} = 10\,\mu A$ at $27^\circ C$ and $h_{fe} = 50$. a) Find I_c when $I_B = 0.25\,mA$ and b) assuming h_{fe} doesnot change with temperature find the value of new collector current, if the transistor's temp. rises to $50^\circ C$.

Sol: Given $I_{CBO} = 10\,\mu A$, $h_{fe}\,(=\beta) = 50$. $I_B = 0.25\,mA$

a) $I_c = \beta I_B + (1+\beta) I_{CBO}$

$= 50 \times (0.25 \times 10^{-3} + (1+50) \times 10 \times 10^{-6}$

$= 13.01\,mA$

b) $I'_{CBO}\,(\beta = 50) = I_{CBO} \times 2^{\Delta T/10}$

$= 10 \times 2^{(50-27)/10}$

$= 49.2\,\mu A$.

$\Rightarrow$ I_c at $50^\circ C$ is

$I_c = \beta I_B + (1+\beta) I'_{CBO}$

$= 50 \times 0.25 \times 10^{-3} + (1+50) \times 49.2 \times 10^{-6}$

$= 16.01\,mA$

$-7mA$ and emitter current equals $7.2mA$. Compute value of α.

Sol: we know that in active region

$$I_C = -\alpha I_E + I_{CBO}$$

if I_{CBO} is neglected.

$$I_C = -\alpha I_E$$

$$\Rightarrow \alpha = -\frac{I_C}{I_E} = -\frac{(-7\times10^{-3})}{7.2\times10^{-3}} = 0.972$$

(Pb) Calculate the value of I_C and I_E for a transistor with $\alpha = 0.99$, $I_{CBO} = 5\mu A$ and $I_B = 20\mu A$.

Sol: Given That $\alpha = 0.99$.

$$\Rightarrow \beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = 99.$$

$$I_C = (1+\beta) I_{CBO} + \beta I_B = \frac{1}{1-\alpha} \cdot I_{CBO} + \frac{\alpha}{1-\alpha} I_B.$$

$$= 100 \times 5\times10^{-6} + 99 \times 20 \times 10^{-6}$$

$$I_C = 2.48\ mA.$$

$$I_E = I_B + I_C = 20\mu + 2.48m = 2.5mA.$$

(Pb) Emitter current in a certain NPN transistor is $8.4mA$. If 99.8% of majority carriers injected into the base - recombine with hole and leakage current at collector is $0.1\mu A$. Find

a) I_B b) I_C c) α d) α_{dc}.

Sol:

$$I_B = 0.8\% \text{ of } I_E$$

$$= \frac{0.8}{100} \times 8.4\times10^{-3} = 67.2\mu A$$

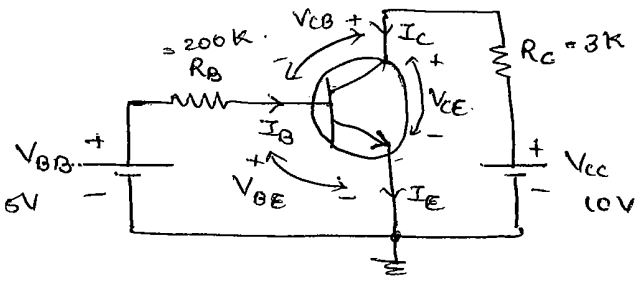
$$I_E = I_B + I_C.$$

$$\Rightarrow I_C = I_E - I_B = 8.4m - 67.2\mu = 8.332\ mA$$

$$\alpha = \frac{I_C - I_{CBO}}{I_E} = \frac{8.332m - 0.1\mu}{8.4m} = 0.9919$$

$$\alpha_{dc} = \frac{I_C}{I_E} = \frac{8.332\times10^{-3}}{8.4\times10^{-3}} = 0.992$$

(Pa) For the following circuit, [illegible] with $\beta = 100$ and $I_{CBO} = 20\,nA$.



Sol: $I_E = F_B$

⇒ assume it is in active region.

Applying KVL to base ckt

$V_{BB} - R_B I_B - V_{BE} = 0$.

$5 - (200K) I_B - V_{BE\,(active)} = 0$.

↳ 0.7V for Si.

$\Rightarrow I_B = \frac{5 - 0.7}{200 \times 10^3} = 21.5\,\mu A$

$V_{CE} = V_{CB} + V_{BE}$ (↑ +ve, ↑ +ve)

⇒ only if V_{CB} is +ve, $I_C = R_B$

for a txor in active region,

$I_C = (\beta) I_B + I_{CBO}(1+\beta)$

$= 100 \times 21.5 \times 10^{-6} + 20 \times 10^{-9} \times 101$.

$= 2.152\,mA$.

from circuit, $I_E = I_B + I_C = 2.152m + 21.5\mu$.

$= 2.1716\,mA$.

Applying KVL to collector circuit via base.

$10 - (3K) \cdot I_C - V_{CB} - V_{BE\,(active)} = 0$.

$V_{CB} = 2.86V$.

V_{CB} is +ve ⇒ collector junction is R.B.

⇒ txor is in active region ⇒ our assumption is correct.

(Pb) The reverse saturation current of a transistor when connected in common base configuration is $0.2\,\mu A$. whereas it is $18\,\mu A$ when connected in common emitter configuration. calculate forward current gain in CB and CE configurations

Sol: $I_{CBO} = 0.2\,\mu A$

$I_{CEO} = 18\,\mu A$

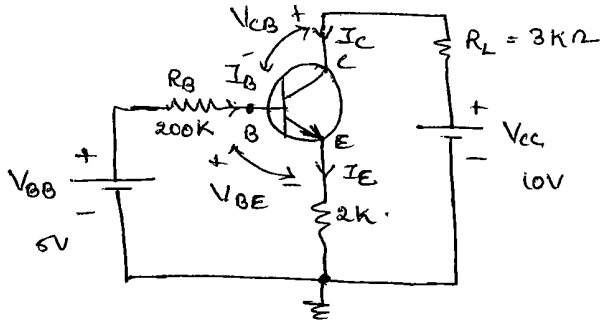
$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha}$.

$I_C = \beta I_B + I_{CEO}$.

$\Rightarrow I_{CEO} = \frac{I_{CBO}}{1-\alpha}$. $\Rightarrow 1-\alpha = \frac{I_{CBO}}{I_{CEO}}$ $\Rightarrow \alpha = 1 - \frac{I_{CBO}}{I_{CEO}} = 0.988$

$\beta = \frac{\alpha}{\quad} = 0.988$

transistor with $\beta = 100$ and $I_{CBO} = 20nA$.



Sol: $I_E = FB$

$\Rightarrow$ It can be active or saturation.

Assume, That trxor as in active region

Applying KVL at base circuit

$$V_{BB} - R_B I_B - V_{BE} - I_E \cdot R_E = 0.$$

$$5 - (200K) I_B - 0.7V - (2K) I_E = 0.$$

for a trxor in active region

$$I_c = I_B \cdot \beta + I_{CBO}(1+\beta).$$

and $I_E = I_B + I_C = (1+\beta) I_B + (1+\beta) I_{CBO}$ neglecting

$$I_E = (1+\beta) I_B.$$

$$= 101 I_B.$$

$$\Rightarrow 5 - (200K) I_B - 0.7 - (2K)(101 I_B) = 0.$$

$$I_B = \frac{5 - 0.7}{(200 + 202) \times 10^3} = 10.69 \mu A$$

$$I_E = 101 \times I_B = 1.08 mA$$

$$I_c = I_E - I_B = 1.069 mA$$

Applying KVL to collector circuit via base.

$$V_{CC} - I_c \cdot R_L - V_{CB} - V_{BE(active)} - R_E \cdot I_E = 0$$

$$10 - (1.069m)(3K) - V_{CB} - 0.7 - (2K)(1.08m) = 0.$$

$$V_{CB} = 3.935V$$

Since V_{CB} = +ve $\Rightarrow$ $I_c = R.B$

$\Rightarrow$ trxor is in active region $\Rightarrow$ our assumption is correct.

(Pb) In a certain transistor, 99.6% of the [illegible] cross the collector-base junction. If the leakage current is 5μA and the collector current is 20mA, calculate.

i) α_{dc} ii) I_E.

Sol: Given $I_c = 0.996\, I_E$, $I_{CBO} = 5\mu A$, $I_c = 20mA$.

$$\alpha_{dc} = \frac{I_c}{I_E} = 0.996. \quad , \quad I_c = \alpha_{dc} \cdot I_E + I_{CBO}$$

$$I_E = \frac{I_c - I_{CBO}}{\alpha_{dc}} = \frac{20m - 5\mu}{0.996} = 20.07\ mA$$

(Pb) Calculate the value of I_c and I_B for a transistor with $\alpha_{dc} = 0.99$ and $I_{CBO} = 10\mu A$. The emitter current is measured as 8mA.

Sol: $\alpha_{dc} = 0.99$, $I_{CBO} = 10\mu A$, $I_E = 8mA$.

$$I_c = \alpha_{dc} I_E + I_{CBO}.$$

$$= 0.99 \times 8 \times 10^{-3} + 10 \times 10^{-6} = 7.93\ mA$$

$$I_B = (1 - \alpha_{dc}) I_E - I_{CBO}.$$

$$= (1 - 0.99) \times 8 \times 10^{-3} - 10\mu = 70\mu A$$

(Pb) If $\beta = 100$, $I_{CBO} = 10\mu A$ and $I_B = 80\mu A$. Find I_E.

Sol: $I_E = I_B + I_c$

$$= I_B + \alpha I_E + I_{CBO}. \qquad \because \beta = \frac{\alpha}{1-\alpha}.$$

$$I_E = \frac{I_B}{1-\alpha} + \frac{1}{1-\alpha} I_{CBO}. \qquad 1+\beta = \frac{\alpha}{1-\alpha} + 1 = \frac{1}{1-\alpha}.$$

$$= (1+\beta) I_B + (1+\beta) I_{CBO}.$$

$$= (1+100) \times 80\mu + (1+100) \times 10\mu. = 9.09\ mA$$

(Pb) If $\alpha = 0.98$, $I_{CBO} = 10\mu A$, $I_B = 100\mu A$. Find I_E.

Sol: $\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$

$$I_E = (1+\beta) I_B + (1+\beta) I_{CBO}$$

$$= 50 \times 100 \times 10^{-6} + 50 \times 10 \times 10^{-6}$$

$$= 5.5\ mA$$

Field Effect Transistors.

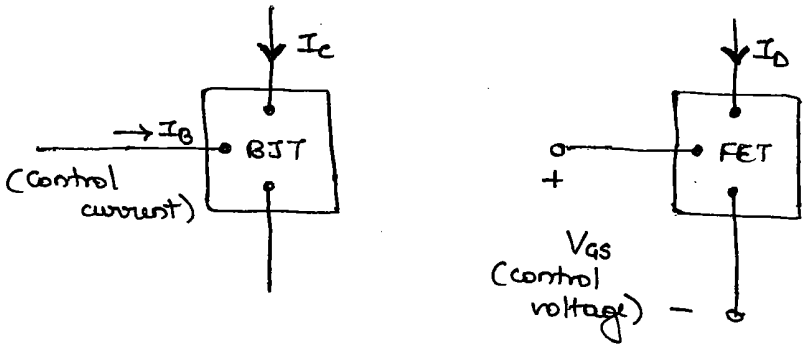
"Electronic Devices & Circuits Theory"
by Robert L Boylestad
Louis Nashelsky.

* Introduction

The field effect transistor (FET) is a 3-terminal device same as BJT. The primary difference between the two types of transistor is the fact that

BJT is **current-controlled device**.

FET is **voltage-controlled device**



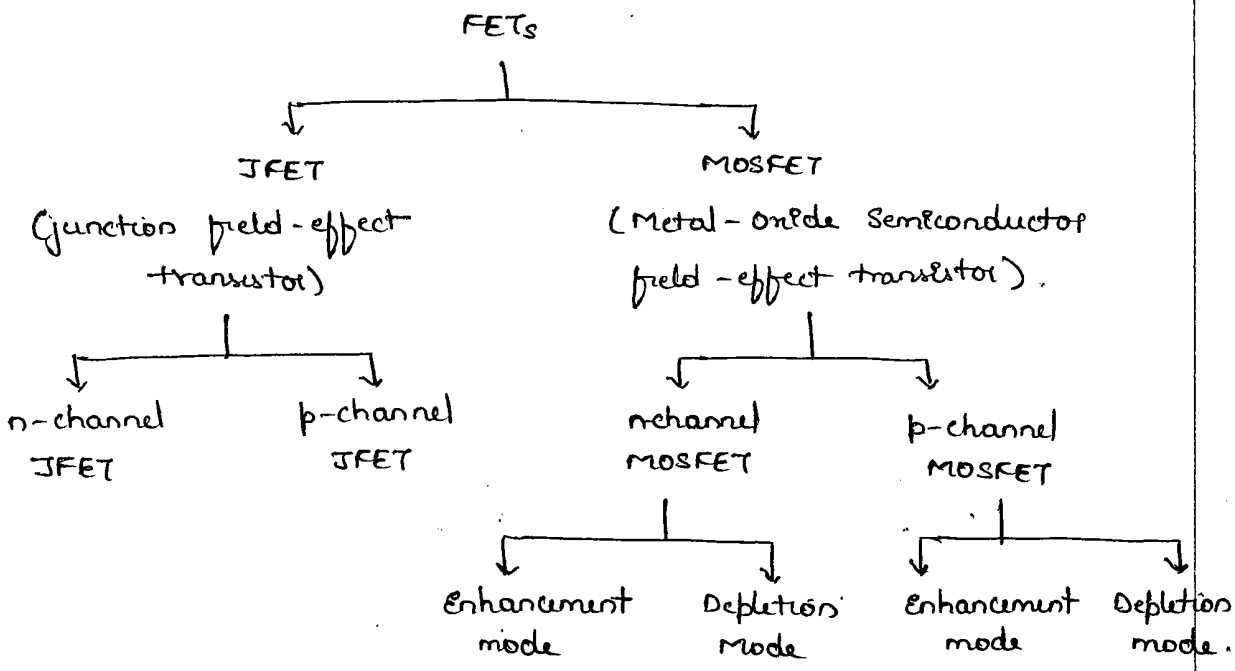
BJT is a **bipolar device**, "bi"- revealing that the conduction level is a function of two charge carriers, electrons & holes. whereas FET is a **unipolar device** depending solely on either electrons (n-channel) or hole (p-channel) conduction.

As permanent magnet has got the ability to draw metal filings to the magnet without the need for actual contact, for FET an electric field established by the charges controlling the conduction path of the output circuit without the need for direct contact between the controlling & controlled quantities. Hence, the name "**field-effect**".

One of the most important characteristic of FET is it has **high-input impedance**, which is very important in the design of linear ac amplifier systems.

In general, FETs are **more temperature stable** than BJT, ~~making~~ ~~them~~ and are **smaller in construction**, making them particularly useful in Integrated-Circuits (IC) chips.

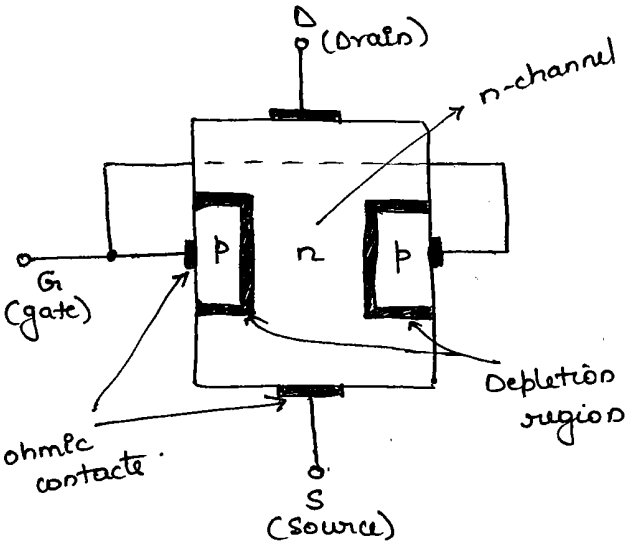
Different types of FETs are.



* MOSFET is also called as IGFET (Insulated Gate Field effect transistor.

JFET is a Three-terminal device with one device terminal capable of controlling the current between the other two terminals.

The basic construction of n-channel JFET is shown

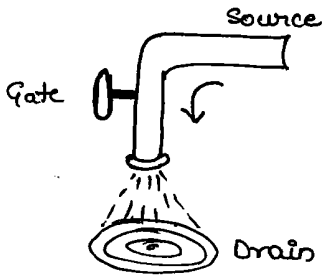


Major part of the structure is the n-type material that forms the channel between the embedded layers of p-type material.

The top of n-type channel is connected through an ohmic contact to a terminal referred to as the **drain (D)**, while the lower end of the same material is connected through an ohmic contact to a terminal referred to as **source (S)**. The two p-type terminals are connected together & referred to as **Gate (G)**

In the absence of any applied potentials the JFET has 2 pn junctions under no-bias conditions. The result is a depletion region at each junction which is same as pn junction diode under no-bias conditions

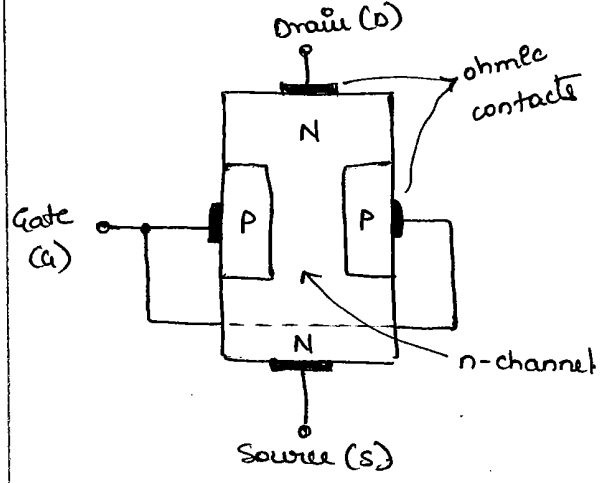
Water Analogy for JFET



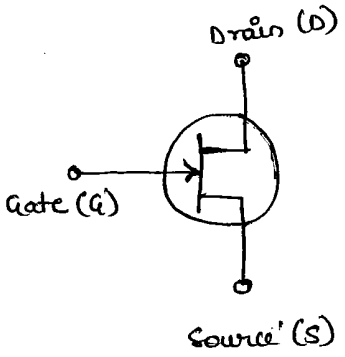
The source of water pressure can be considered as applied voltage from source to drain that will establish a flow of water (electrons) from the spigot (source).

The "gate" through an applied signal (potential), controls the flow of water (charge) to the "drain".

* Structure & symbol of n-channel JFET

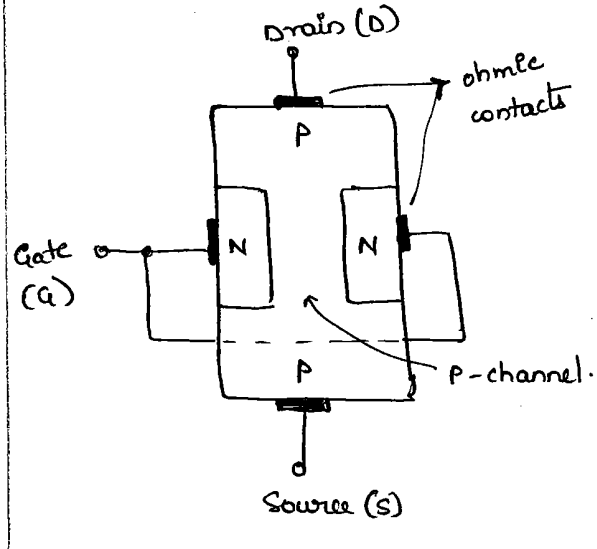


a) Structure

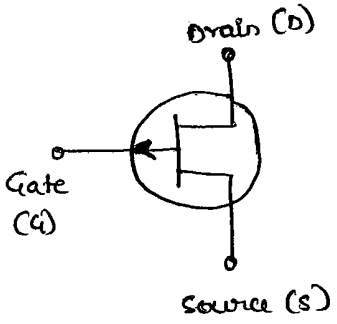


b) Symbol

* Structure and symbol of p-channel JFET



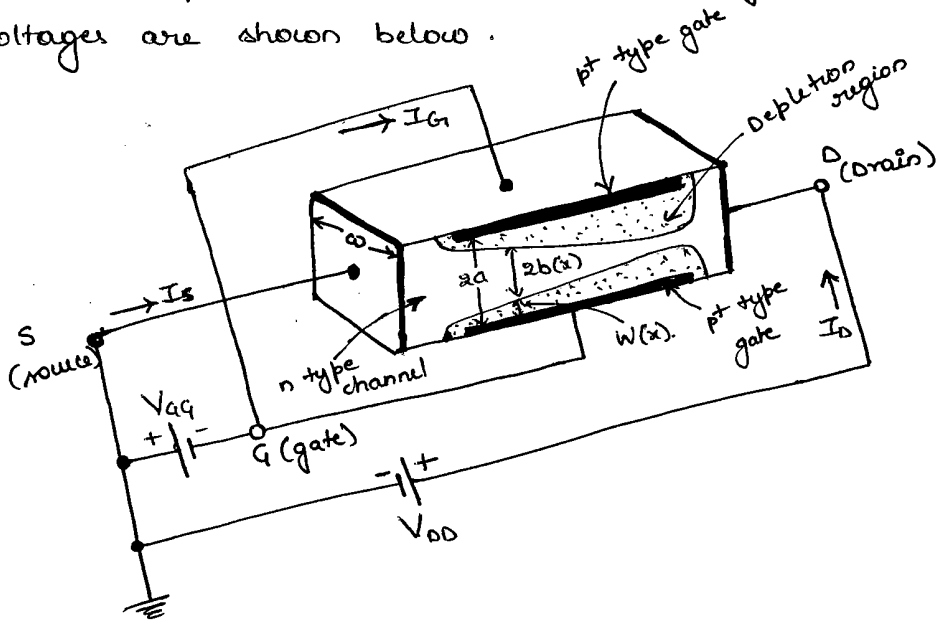
a) Structure



b) Symbol.

The arrow mark on the gate terminal shows the direction of flow of current when gate junction is forward biased.

The basic structure of n-channel JFET with its normal polarities for drain-to-source and gate-to-source supply voltages are shown below.

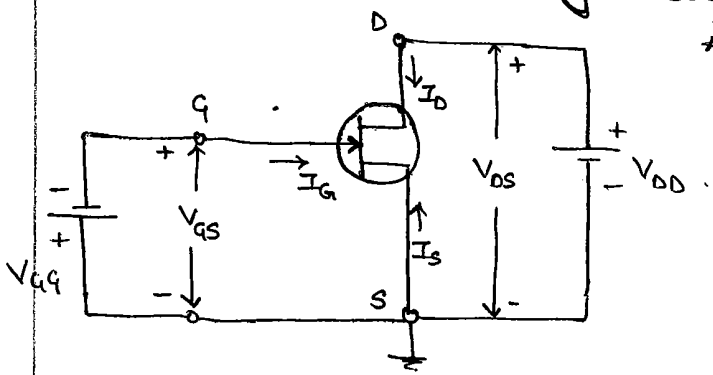


As the reverse bias across the junction increases, the thickness of the depletion region also increases. The conductivity of the depletion region is normally zero because of the unavailability of charge carriers. ⇒ Effective width of channel will progressively decrease with increasing reverse bias as shown above.

Accordingly, for a fixed drain-to-source voltage, the drain current will be a function of the reverse-biasing voltage across the gate junction.

The term **field effect** is used to describe this device because the mechanism of current control is the effect of field associated with the region of uncovered charges which is due to applied reverse bias.

∴ Hence, FET is **voltage controlled device**



Common-source configuration

*** for n-channel

I_D, V_{DS} = +ve.

V_{GS} = −ve

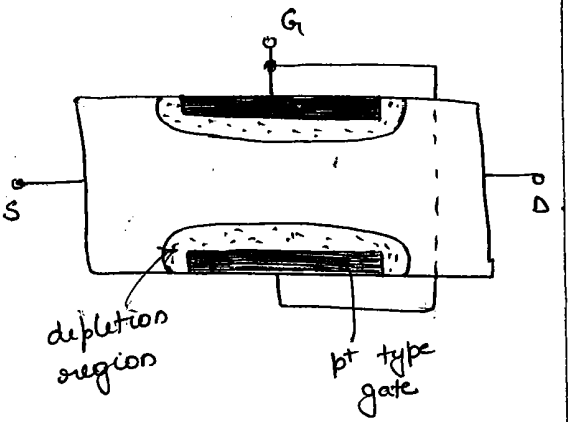
*** for p-channel.

I_D, V_{DS} = −ve

V_{GS} = +ve.

In common source configuration, gate is connected to negative supply and drain to positive supply, such that the charge carriers electrons enter through source and leave through drain.

Case (a): when $V_{DS}=0$ and $V_{GS}=0$.



when $V_{DS}=0$ and $V_{GS}=0$, the thickness of depletion region around the pn junction is uniform as shown.

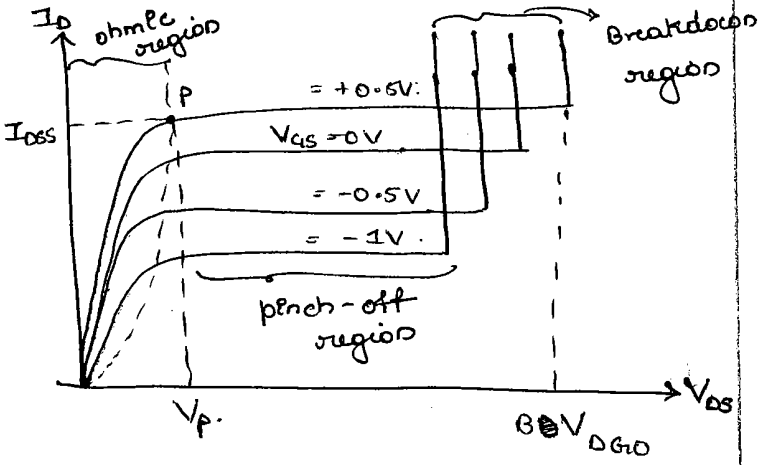
The depletion region penetrates more into the channel since gates are heavily doped.

Case (b): when $V_{GS}=0$ and V_{DS} is increased.

As V_{DS} is increased, drain is positive wrt source and hence the majority charge carriers (electrons) flow through the N-channel from source to drain ⇒ conventional current I_D flows from drain to source.

Initially as V_{DS} increases, I_D increases and this region is called **ohmic region** as shown in the drain characteristics below.

For the gate-to channel junction (P^+N junction), n channel is connected to +ve supply
⇒ gate-to-channel is reverse biased.



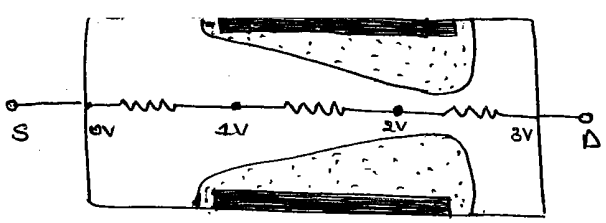
Drain characteristics

As $V_{DS}\uparrow$, reverse bias increases and depletion region width increases. It is seen that the penetration of depletion region is unequal. It penetrates more that the drain side than at the source side as shown below.

i.e it takes a **wedge shape**

The channel can be assumed as a semiconductor resistor,

$$R = \frac{\rho L}{A}$$



where ρ = resistivity of channel

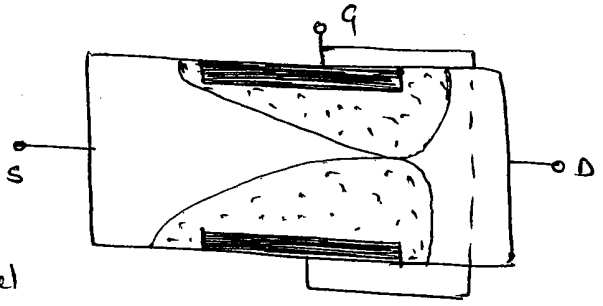
L = length of channel.

A = cross-sectional area.

Across the length of the channel towards the drain side, "L" increases. ⇒ voltage drop at drain side increases since same current (I_D) is flowing in the channel. ⇒ voltage drop across the channel is variable.

Due to the large voltage drop at drain side, the gate channel pn junction diodes get more reverse biased at drain-side compared to source-side ⇒ shape of the depletion region is wedge-shaped

As V_{DS} increases, depletion region penetrates more into the channel and at some point it closes the channel near the drain side as shown below.



The effective channel height $2b(x)$ decreases.

This situation is called **pinch off**. At this voltage, channel is said to be pinched off and the drain voltage V_p is called as **pinch-off voltage**.

After V_p, if V_{DS} is further increased, I_D doesnot increase and remains constant. This region in drain characteristics is called **constant current region** or **saturation region**.

If V_{DS} is further increased, due to avalanche **multiplication** or **breakdown**, drain current drastically increases as shown in drain characteristics.

case (c) :- when V_{GS} = -ve and V_{DS} is increased.

when V_{GS} = -ve and V_{DS} is increased, Thus width of depletion region with V_{DS} = 0 is greater than width of depletion region for V_{GS} = 0. Due to more width of depletion region initially, pinch off and breakdown occurs at lower values of V_{DS} compared to values with V_{GS} = 0.

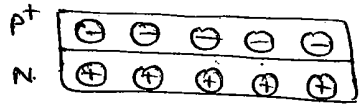
case (d) :- when V_{GS} = +ve and V_{DS} is increased

when V_{GS} = +ve, width of depletion region decreases ~~that~~ below open circuit case. Hence, at larger values of V_{DS} pinch off and break down occurs lately as shown in drain characteristics.

For different values of V_{GS} the drain characteristics exhibit different slopes (resistances) in ohmic region. Hence, JFET can be used as **voltage variable resistor (VVR)** or **voltage dependent resistor (VDR)**

As V_{GS} increases the depletion region penetration into channel increases. Hence, effective channel height decreases. $\Rightarrow I_D \downarrow$
i.e voltage applied to the gate is controlling o/p current.
Hence, JFET is called **voltage controlled device**.

In the depletion regions of p^+ and N junctions, immobile ions get developed as shown



The electric flux lines developed between the +ve and -ve charges are controlling the output. Hence, this device is called **field effect transistor**

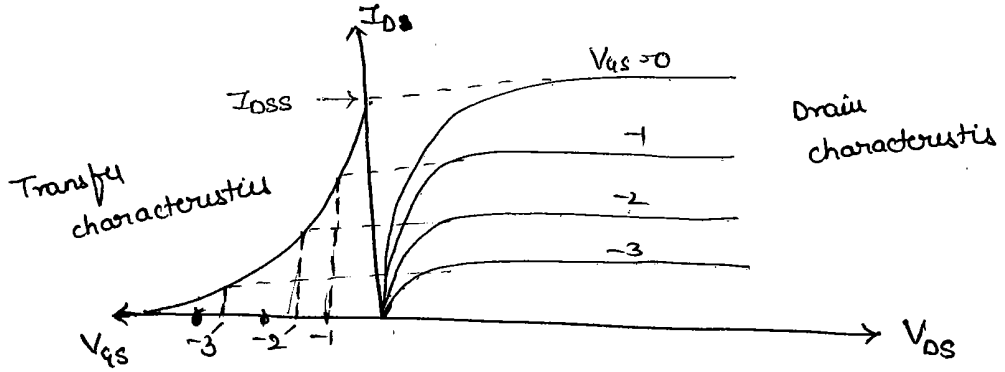
The ~~of~~ electric field developed across the junctions (p^+N) of gate is controlling the overall operation, hence called as **Junction field effect transistor**.

For JFET output characteristics are drawn between drain current (I_D) and drain voltage (V_{DS}), and they are called as drain characteristics.

The input characteristics are generally not drawn because input current (I_G) is small or zero due to i/p voltage V_{GS} being -ve.

Hence, for JFET transfer characteristics are drawn with one o/p variable (I_D) and one i/p variable (V_{GS}).

The following graph shows transfer characteristics I_D Vs V_{GS} derived from drain characteristics.



It is seen that the characteristics look like a parabola & hence it can be approximated using the following equation

$$I_{DS} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

where I_{DS} = saturation drain current

I_{DSS} = value of I_{DS} when $V_{GS} = 0$.

V_P = pinch off voltage.

* Characteristic parameters of JFET:

In a JFET, the drain current I_D depends up drain voltage V_{DS} and the gate voltage V_{GS}. Any one of them may be fixed and the relation between other two are determined. These relations are determined by the three parameters which are defined below

a) Mutual conductance or Transconductance (g_m)

It is the slope of transfer characteristics curve and is defined as

$$g_m = \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}\ =\ \text{constant}}$$

b) Drain resistance (r_d)

It is the reciprocal of the slope of the drain characteristics and is defined as

$$r_d = \left(\frac{\partial V_{DS}}{\partial I_D}\right)_{V_{GS}} = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}\ =\ \text{constant}}$$

The reciprocal of r_d is called drain conductance denoted by g_d.

c) Amplification factor (μ)

It is defined as

$$\mu = -\left(\frac{\partial V_{DS}}{\partial V_{GS}}\right)_{I_D} = \left.-\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D\ =\ \text{constant}}$$

* Relationship among FET parameters

As I_D depends on V_{DS} and V_{GS}, the functional equation is

$$I_D = f(V_{DS}, V_{GS})$$

$$\Delta I_D = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \cdot \Delta V_{DS} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} \cdot \Delta V_{GS}$$

$$\Rightarrow \frac{\Delta I_D}{\Delta V_{GS}} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \cdot \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right) + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

If I_D = constant $\Rightarrow \frac{\Delta I_D}{\Delta V_{GS}} = 0 \Rightarrow 0 = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right)_{I_D} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$

$\Rightarrow 0 = \left(\frac{1}{r_d}\right)(-\mu) + g_m \Rightarrow$

* Comparison of FET and BJT

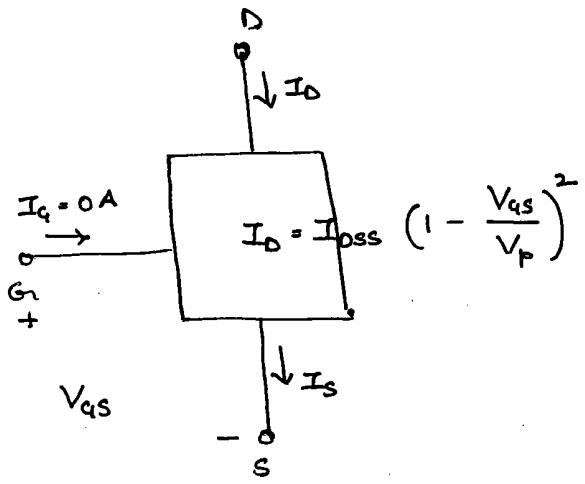
1. FET operation depends only on the flow of majority carriers (holes for p-channel and electrons for n-channel). Hence called as unipolar device. whereas BJT's operation depends on both minority and majority current carriers. Hence called bipolar devices.
2. In the path of current flow, There are no junctions in FET where as BJT's have 2 junctions. ⇒ FET is less noisy than BJT.
3. As the i/p circuit of FET is reverse biased, FET exhibits a much higher i/p impedance (≈ 100MΩ) and lower o/p impedance and There will be a higher degree of isolation b/w i/p and o/p. ⇒ FET acts as an excellent buffer amplifier but the BJT has low i/p impedance because its i/p circuit is forward biased.
4. FET is a voltage controlled device i.e voltage at i/p terminal controls the o/p current, whereas BJT is current controlled device, i.e i/p current controls o/p current.
6. FETs are much easier to fabricate and are particularly suitable for IC's because They occupy less space Than BJT.
6. Effect of temperature on performance of FET is less than That of BJT (no thermal runaway in FET).
7. FET doesnot suffer from minority carrier storage effect. Hence, it has higher switching speed and cut-off frequencies compared to BJT.

* Comparison of "n" with "p" channel JFET

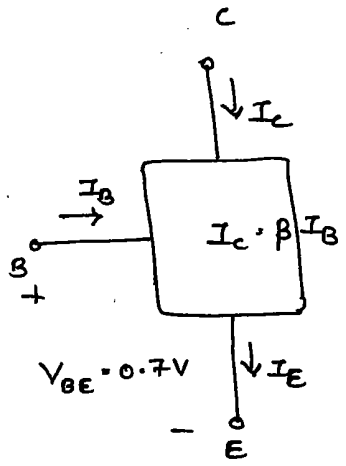
1. In n-channel current drives are electrons and in p-channel current carriers are holes.
2. Mobility of electrons is large when compared to holes.
3. i/p noise is less for n-channel when compared to p-channel JFET.
4. Transconductance is large in n-channel Than in p-channel JFET

* Applications of JFET.

1. Used as buffer in measuring instruments, since it has high i/p impedance & low o/p impedance.
2. Used in RF amplifiers in FM tuners & communication equipment for the low noise level.
3. Since the device is voltage controlled device, it is used as voltage variable resistor in operational amplifiers.
4. Used as oscillator because frequency drift is low.
5. Used in digital circuits because of its small size.
6. Used as switch.



a) JFET



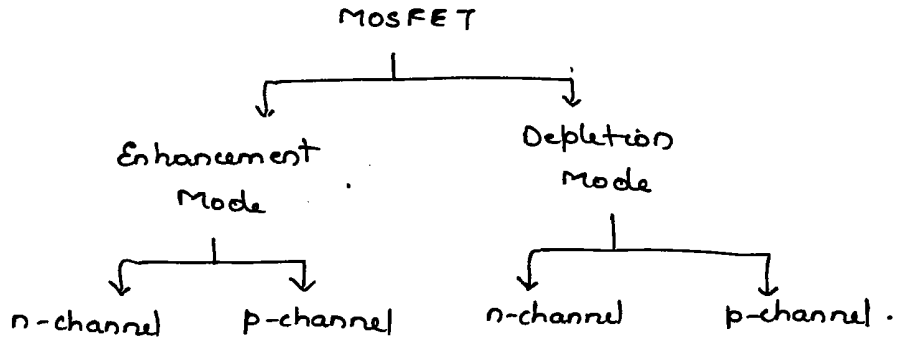
b) BJT

(1) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)$ $\Longleftrightarrow$ $I_C = \beta I_B$.

(2) $I_D = I_S$ $\Longleftrightarrow$ $I_C \cong I_E$

(3) $I_G \cong 0A$ $\Longleftrightarrow$ $V_{BE} \cong 0.7V$.

Important relationships.



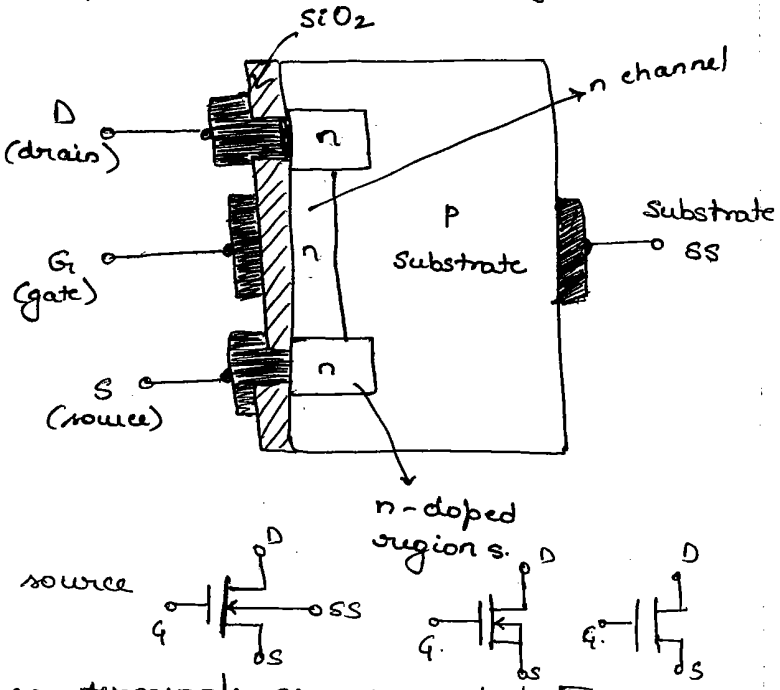
* Depletion type MOSFET :

a) Basic construction of n-channel MOSFET.

The basic construction of n-channel depletion-type MOSFET is shown below.

A slab of p-type material is formed from a silicon base and is referred to as the substrate.

It is the foundation on which the device is constructed. In general, substrate is connected to source terminal internally.



The drain & source terminals are connected through metallic contacts to n-doped regions linked by an n-channel

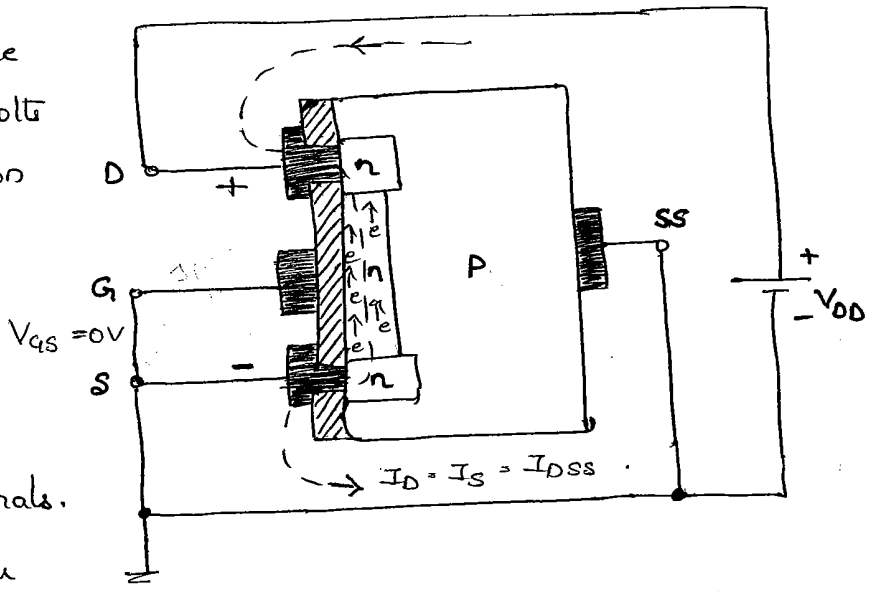
The gate is also connected to a metal contact surface but remains insulated from n-channel by a very thin silicon dioxide (SiO_2) layer.

Since, There is no direct electrical connection b/w gate terminal & channel of MOSFET, i/p impedance is very high, which supports the fact that $I_G = 0$ for dc-biased conditions.

Since, gate, source and drain are connected through metallic contacts, Then SiO_2 is acting as insulating material b/w gate & channel & semiconductor is used as substrate, The

→ Case (a): $V_{GS} = 0V$ and V_{DS} = +ve.

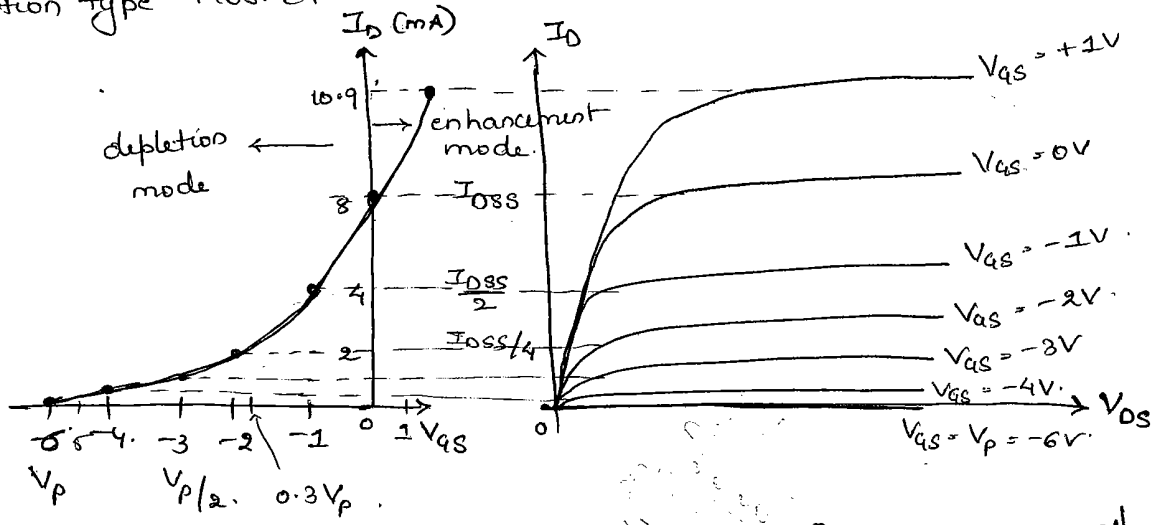
The gate to source voltage is set to 0 volts by the direct connection from one terminal to the other, and a voltage V_{DS} is applied across the drain to source terminals.



The result is an attraction for the positive potential at the drain by the free electrons of the n-channel and current is established. Through the channel

At $V_{GS} = 0$, drain current $I_D = I_{DSS}$.

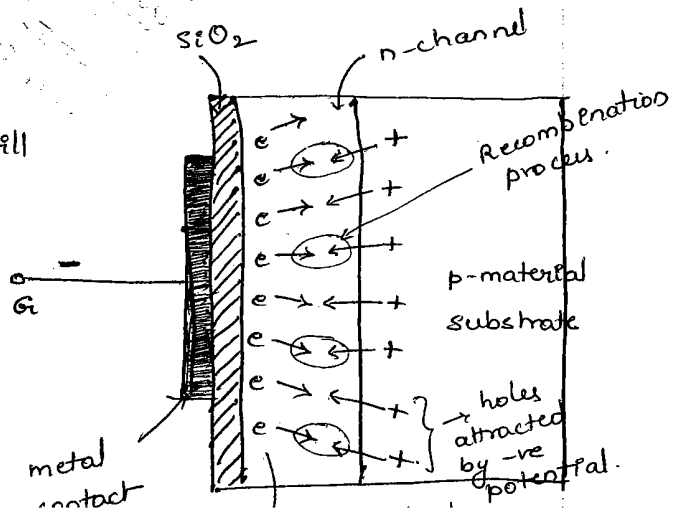
The drain and transfer characteristics for an n-channel depletion type MOSFET as shown below



→ Case (b): V_{GS} = −ve such as −1V

The negative potential at the gate will tend to pressure electrons towards the p-type substrate and attract holes from p-type substrate.

Depending upon the magnitude of negative bias, a level of



n-channel available for conduction.

The more the negative bias, the higher the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS} as shown in figure for $V_{GS} = -1V, -2V$ and so on, to the pinch off level of $-6V$.

→ case (c): V_{GS} = +ve say 1V.

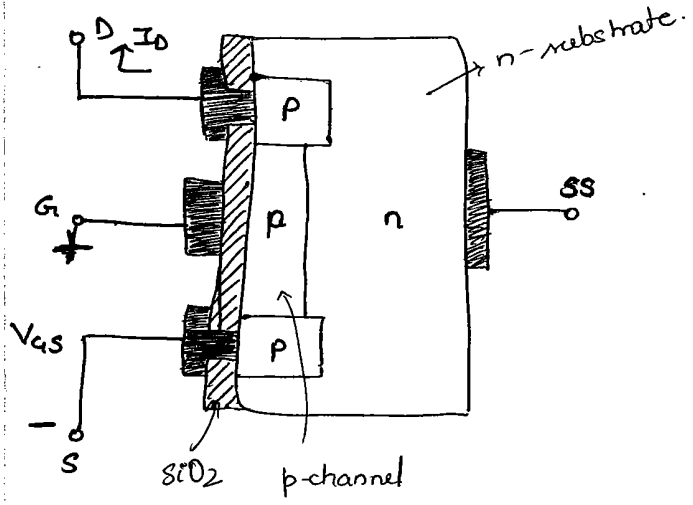
For positive values of V_{GS}, the positive gate will draw additional electrons from the p-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles.

As, V_{GS} continues to increase in the positive direction, the drain current will increase at a rapid rate.

The application of positive V_{GS} has "enhanced" the level of free carriers in the channel compared to the one that $V_{GS} = 0V$.

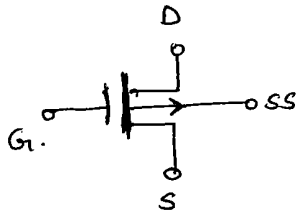
⇒ The region of positive gate voltages on the drain or transfer characteristics is often referred to as "enhancement region". with the region between cutoff and saturation of I_{DSS} is referred to as "depletion region".

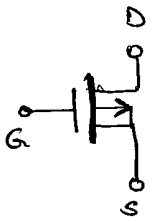
c) P-channel depletion-type MOSFET

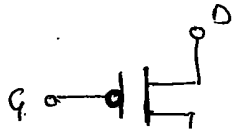


construction of p-channel depletion type MOSFET is exactly the reverse of n-channel.

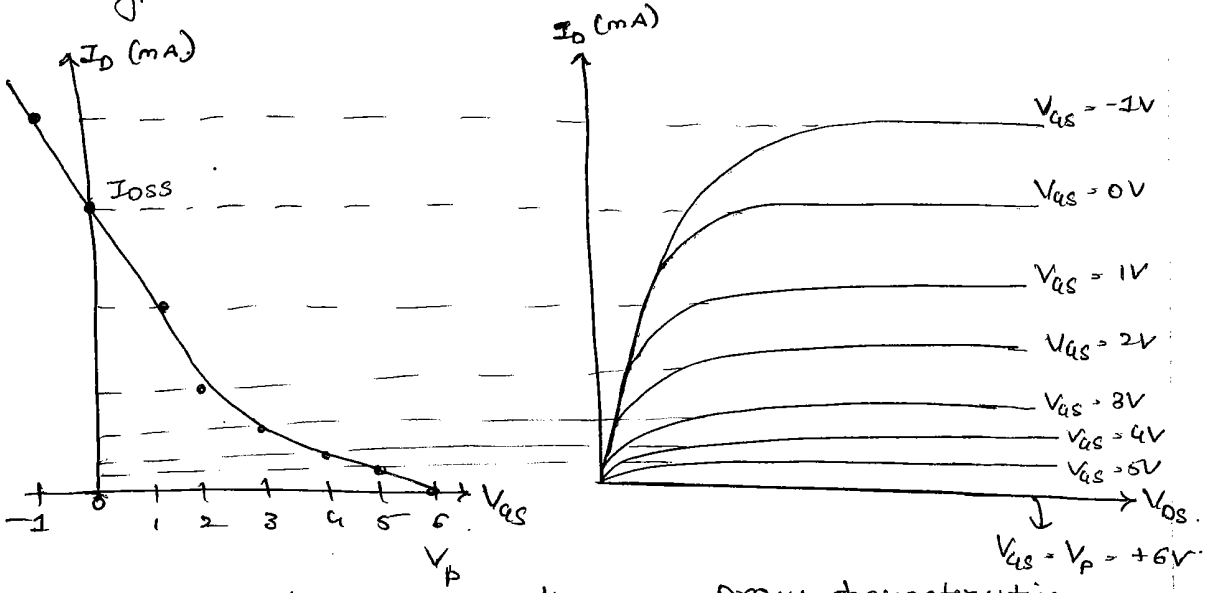
Here, Substrate = n type.
Channel = p type.







depletion type MOSFET as shown below.



Transfer characteristics Drain characteristics

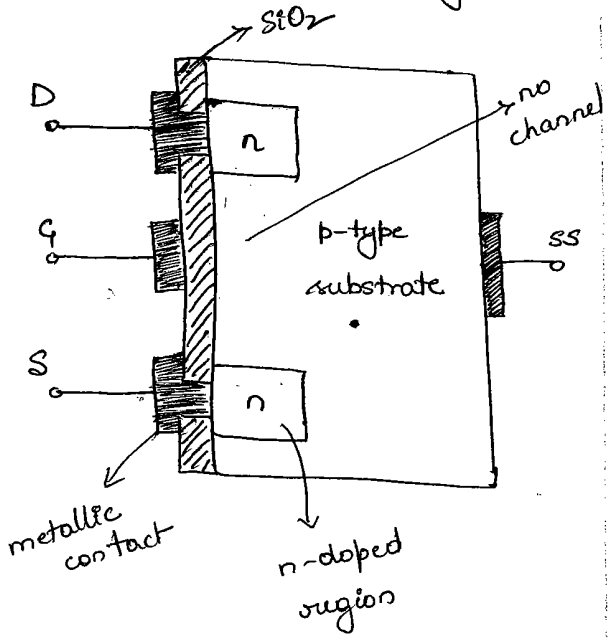
* Enhancement type MOSFET

a) Basic construction

The basic construction of the n-channel enhancement-type MOSFET is provided below

Primary difference between enhancement & depletion type MOSFET's is absence of a channel between the two n-doped regions, in enhancement type.

Rest of the construction is same for both enhancement & depletion type MOSFETs.

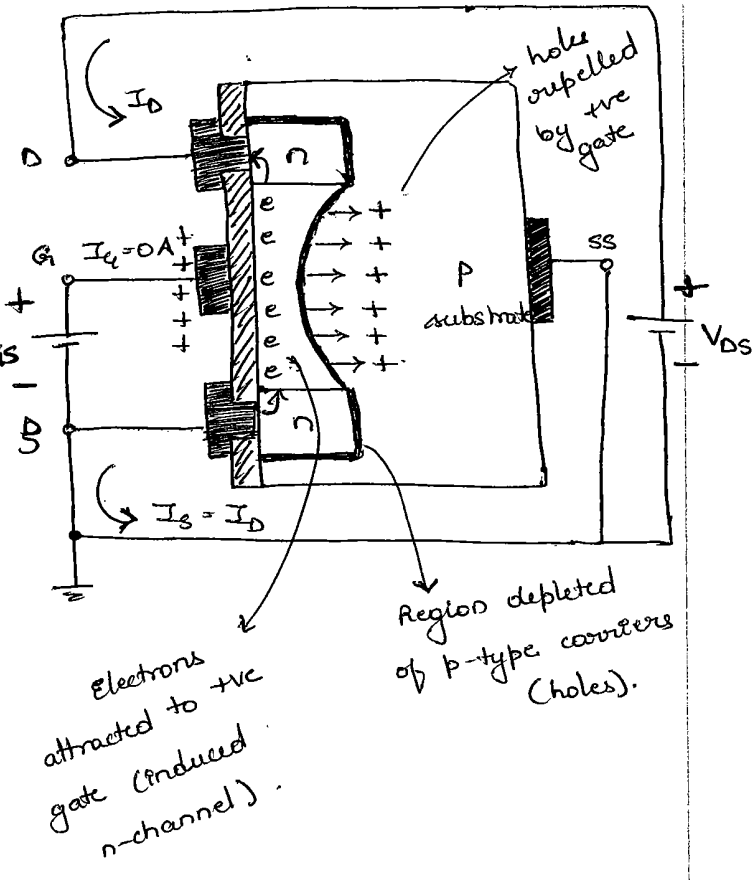


b) Basic operation & characteristics.

→ If $V_{GS} = 0V$ and a voltage is applied between drain & source, the absence of n-channel will result in 0 current.

(But for depletion regions at $V_{GS} = 0$, $I_D = I_{DSS}$)

The positive potential at the gate will pressure the holes in the p-substrate along the edge of SiO_2 layer to leave the area & enter deeper regions of p-substrate. The result is depletion region near SiO_2.



However, electrons in the p-substrate (minority carriers will be attracted to the positive gate & accumulate near the surface of SiO_2

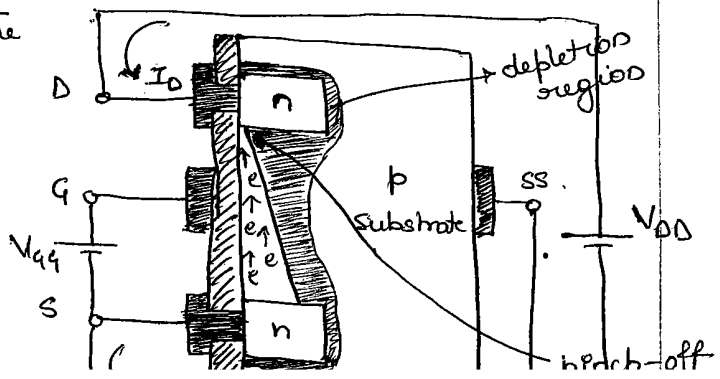
As V_{GS} ↑, concentration of electrons near SiO_2 surface increases until the induced n-type region can support a measurable flow between drain & source.

The level of V_{GS} that results in significant increase in drain current is called Threshold voltage, V_T.

Since channel is nonexistent with $V_{GS} = 0V$ and "enhanced" by the application of a positive gate-to-source voltage, this type of MOSFET is called Enhancement type MOSFET.

As V_{GS} is increased beyond V_T, density of free carriers increases resulting in increase in drain current I_D.

→ If V_{GS} is held constant & V_{DS} is increased, drain current will eventually reach saturation level as in JFET, due to pinch-off process depicted by the



Applying KVL, to the terminal voltages of MOSFET.

$$V_{DG} = V_{DS} - V_{GS}$$

If V_{GS} is held constant @ 8V, and V_{DS} is increased from 2V to 6V,

$$V_{DG} = V_{DS} - V_{GS} = 2 - 8 = -6V$$

$$\cdot \quad = 5 - 8 = -3V.$$

$\Rightarrow V_{DG}$ will drop from $-6V$ to $-3V$ $\Rightarrow$ gate will become less and less positive wrt drain.

This reduction in gate-to-drain voltage will in turn reduce attractive forces for free carriers (electrons) in the region of induced channel; causing reduction in effective channel width.

Eventually, the channel will be reduced to the point of pinch-off and a saturation condition will be established.

$$V_{DS(sat)} = V_{GS} - V_T.$$

** For values of V_{GS} less than V_T, the drain current of an enhancement type MOSFET is 0mA.

for $V_{GS} > V_T$,

$$\boxed{I_D = K (V_{GS} - V_T)^2.}$$

where K = constant $= \dfrac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$

substituting $I_{D(on)} = 10mA$

$V_{GS(on)} = 8V.$ and $V_T = 2V.$

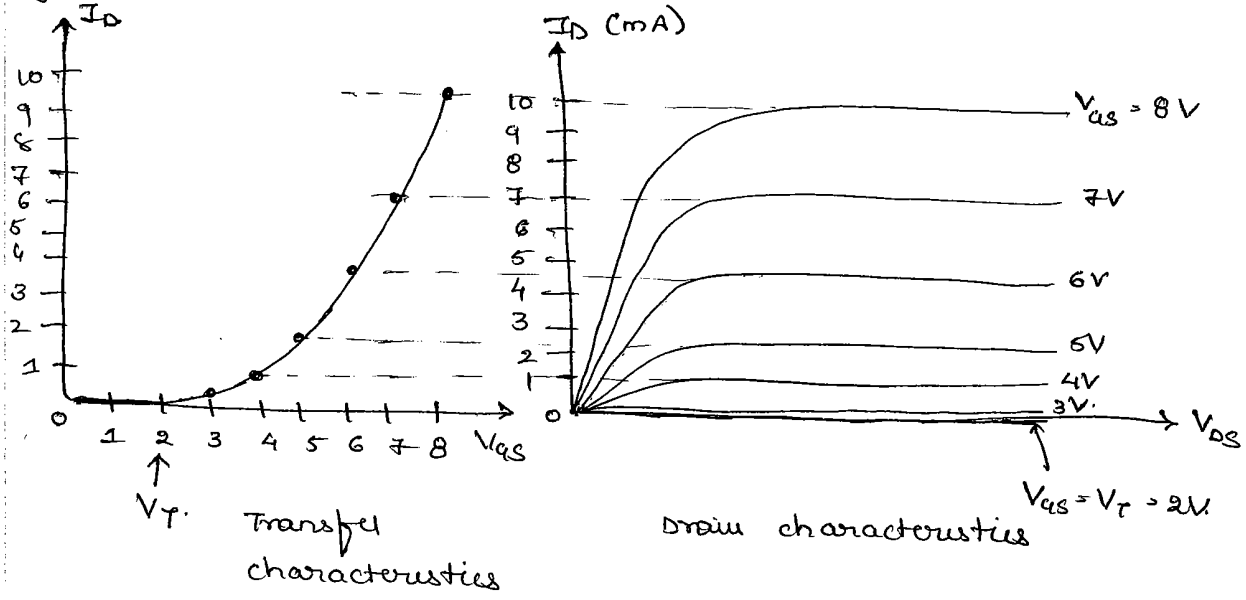
$$K = \frac{10mA}{(8V-2V)^2} = \frac{10mA}{(6V)^2} = 0.287 \times 10^{-3} \, A/V^2.$$

general equation is

$$\boxed{I_D = 0.287 \times 10^{-3} (V_{GS} - V_T)^2}$$

... drain transfer characteristics of ... channel ...

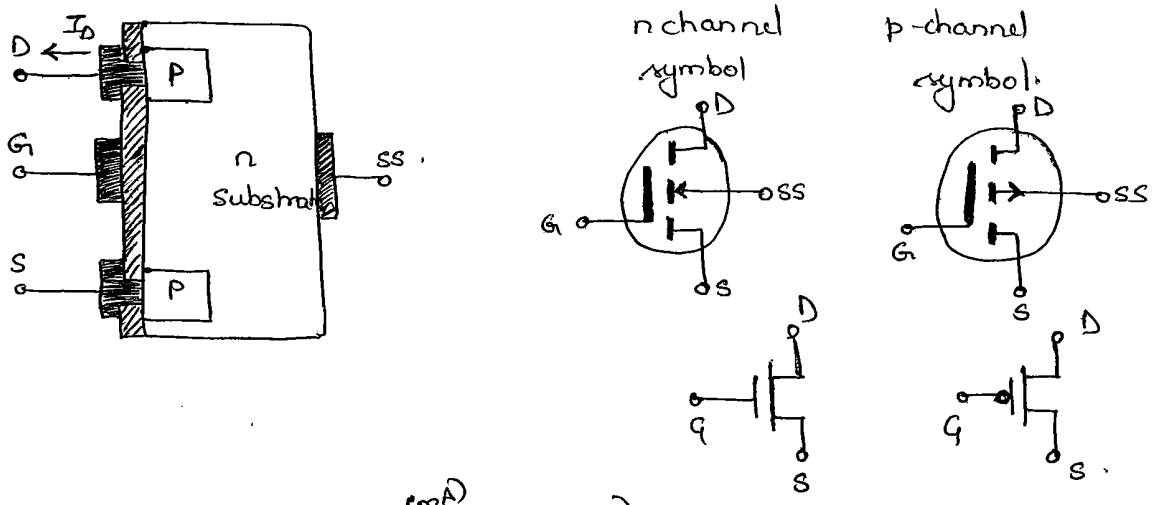
type MOSFET are shown below.

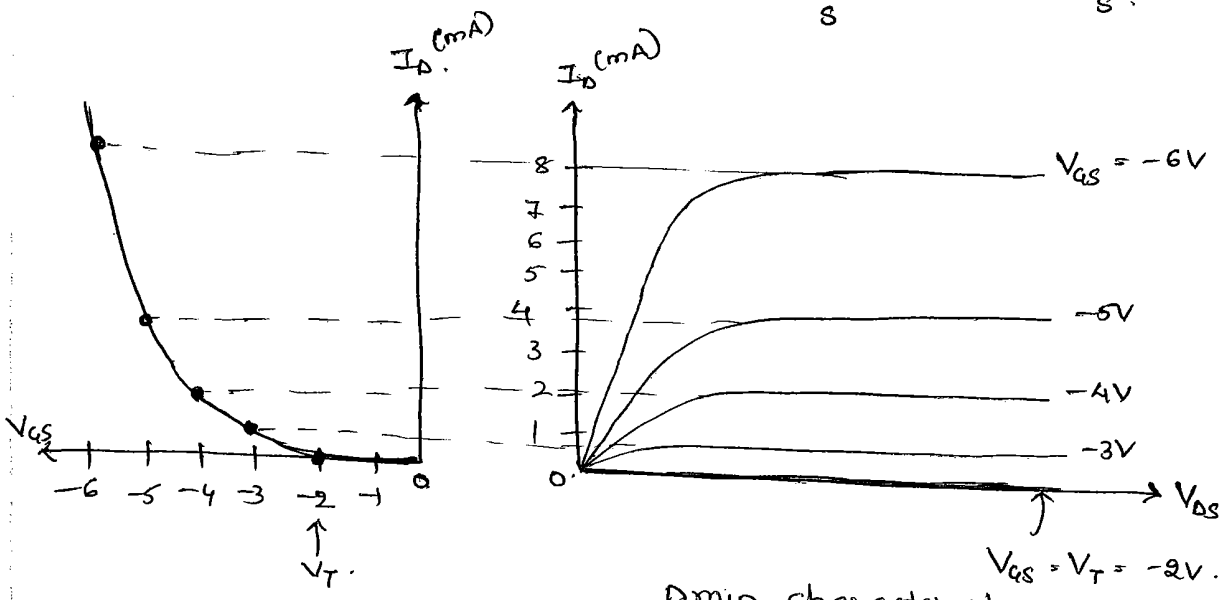


Transfer characteristics

Drain characteristics

c) p-channel enhancement type MOSFET





Transfer characteristics

Drain characteristics

1. In MOSFET, the transverse electric field induced across an insulating material deposited on the semiconductor material controls the conductivity of the channel.

In JFET, transverse electric field across the reverse biased PN junction controls the conductivity of channel.

2. The gate leakage current in a MOSFET is of the order of 10^{-12} A. Hence, the i/p resistance of a MOSFET is very high in the order of 10^{10} to $10^{15}\,\Omega$.

The gate leakage current of a JFET is of the order of 10^{-19} A and its i/p resistance is of the order of $10^{8}\,\Omega$

3. The o/p characteristics of JFET are flatter than those of MOSFET and hence, the drain resistance of a JFET (0.1 to 1MΩ) is much higher than that of MOSFET (1 to 50KΩ).

4. JFET's are operated only in the depletion ~~region~~ mode. MOSFETs are operated in both enhancement & depletion mode.

5. The Fabrication of MOSFET is easier than JFET.

6. MOSFET has zero offset voltage. As it is a symmetrical device, the source and drain can be interchanged. These two properties are very useful in analog signal switching.

7. Special digital CMOS circuits are available which involve near zero power dissipation and very low voltage and current requirements. This makes them more suitable for portable equipments.

8. MOSFETs are very highly susceptible to overload voltage & needs special handling during installation. It gets damaged easily if it is not properly handled.

MOSFETs are widely used in VLSI circuits because of their advantages of over JFET.

a) NMOS advantages.

1. Electron mobility in a given semiconductor material is greater than hole mobility. Hence, N-channel on resistance is less than p-channel on resistance for equal dopings.
2. If on resistance of p-channel is to be made equal with that of on resistance of n-channel then on an average double area is required for p-channel than n-channel.
3. N-channel MOSFET is faster in switching applications due to smaller junction areas. (Internal capacitances are directly proportional to junction areas).
4. NMOS has higher package density.
5. NMOS devices are TTL compatible since the applied gate voltage and drain voltage are positive.

b) PMOS advantages.

1. PMOS is easier & cheaper to fabricate.
2.