A

Project Report On

Implementation of Variable Width Radix-4 Booth Multiplier Using Data Scaling Technology

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VLSI SYSTEM DESIGN

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CERTIFICATE

This is to certify that the dissertation entitled "**Implementation of Variable Width Radix-4Booth Multiplier Using Data Scaling Technology**" is being carried out by **Shivagouni Kalyani** bearing Roll Number **208R1D5707** in partial fulfilment of the academic requirements for the award of the degree of **MASTER OF TECHNOLOGY** in **VLSI SYSTEM DESIGN** for the year 2021-22 submitted to the Department of ELECTRONICSAND COMMUNICATON ENGINEERING, **CMR ENGINEERING COLLEGE UGC AUTONOMOUS**, HYDERABAD.

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ABSTRACT

Multipliers are the basic building blocks in various digital signal processing applications such as convolution, correlation, and filters. However, conventional array multipliers, vedic multipliers were resulted in higher area, power, delay consumptions. Therefore, this work is focused on design and implementation of variable width Radix-4 booth multiplier using Data Scaling Technology (DST). The partial products were generated using radix-4 modified booth encoding. Further, the partial products bits are added using recoding adder in parallel manner with reduced stages. The simulation revealed that the proposed DST-Radix-4 booth multiplier (DST-R4BM) resulted in superior performance in terms of area, delay, power as compared to conventional multipliers.

CHAPTER 1

INTRODUCTION

Reduced vigilance is one of the most important design considerations for practically any electronic system, but it is especially important for mobile electronic devices like mobile phones, tablets, and other electronic devices. To attain this minimal output (speed) penalty, it is essential to do it incredibly quickly. Digital Signal Processing Blocks, sometimes known as DSP for short, are essential components that are used in the manufacturing of a variety of communication systems for mobile devices. The arithmetic and logic operations make up the core of the computing process and provide the majority of multipliers for all of the operations that are carried out on DSP systems. The enhancement of the speed of the multiplier as well as the addition of power- and energy-efficient features plays a significant role in the development of processor efficiency.

A great number of DSP core devices include audio and video algorithms, with the final outputs being created for animal feed in the form of still images or video clips. This makes it easier to utilize estimates to speed up the process of changing energy use. This is due to the low visual capacity of humans, which makes it difficult for them to perceive pictures or recordings. In contrast to the framework that is based on image processing, this framework incorporates a large number of domains in which the correctness of the mathematical functions does not have a major influence on the efficiency of the device. Due to the fact that the model is willing to make use of approximated computing, it is able to provide a selection of levels of accuracy, speed, and overall energy consumption.

Used to imitate the arithmetic units, the loop, and logic, but instead architectural design levels as well as algorithms and software layers may adopt various degrees of design depending on the needs of the application. Abstraction. Estimation can be accomplished through the use of a variety of techniques, including the sanctioning of timing abuses (like raising the voltage or overclocking), feature approximations (like changing a portion of the circuit using the boolean method), and variations. Other techniques include the authorizing of variations. The study of feature approximations on different levels of architecture has seen the introduction of a wide range of approximating arithmetic

fundamental components, including adders and multipliers, among other similar components. For error-tolerant DSP applications, our team is developing a high-speed multiplier with a low energy consumption. The proposed, especially space-efficient approximated multiplier is constructed by modifying the traditional algorithm multiplication approach to assume round input values. This results in the multiplier using much less space.

1.2 PROBLEM STATEMENT

In digital signal processing (DSP) approaches, multipliers are used rather often. These techniques include discrete cosine transform (DCT) [1] and rapid Fourier transform [2], as well as finite impulse response filters [3]. [1] [2] [3] For a good number of years, people have been debating the issue of whether or not digital signal processing (DSP) systems need an easy-to-use yet accurate fixed-width multiplier. The Baugh–Wooley (BW) array multiplier [4]–[6] and the Booth multiplier [7]–[16] are two of the most common varieties of fixed-width multipliers. Because the Booth encoder cuts down on the amount of truncated partial products, multipliers that use the Booth encoder have a greater degree of precision than those that use the BW encoder [12]. A simulation and the statistical likelihood of a low-error fixed-width Booth multiplier are used to arrive at an estimate for the compensating bias of truncated partial products (FWBM). The use of simulation-based error compensation in FWBMs is an approach that yields correct results; nevertheless, the design of its circuits takes a lot of effort. In order to obtain continuous compensation in FWBMs, Jou et al. [7] retrieved the statistical characteristics from a simulation and utilized linear regression. In order to provide adaptive compensation and eliminate truncation error, Song et al. [8] used a curve-fitting approach. In a similar fashion, an exhaustive simulation was used in the circuit that was used in [9] to establish a comparison algorithm, and Wang et al. [10] used additional product information to improve the accuracy; however, establishing an exhaustive simulation is time consuming, particularly for long-width multiplication; despite the fact that exhaustive simulation achieves accurate compensation, establishing an exhaustive simulation takes up a lot of time.

CHAPTER 2

MULTIPLER

2.1 Introduction to Multiplier

The multipliers that shape the primary components of the majority of high-performance devices, such as FIR filters, microprocessors, optical signal processors, etc., are used. Written arithmetic is an example of a difficult procedure. When multiplying without first obtaining authentication, the number must not be taken into consideration. Because the sign number is in the form of a 2, the same procedure cannot be used in signed multiplication. If it were, the result would be incorrect because it is similar to but not the same as the result of non-signed multiplication.

2.2 MULTIPLIER

The process of multiplication is a logical operation that provides the most straightforward method for applying a number to itself a certain number of times. A result (product) is formed by repeatedly applying a number (the multiplicand) to itself in accordance with the parameters set by another number (multiplier). In high school, students learn to subtract by raising the multiplier on account of the generator as part of their instruction. After then, the trustworthy biometric is increased by each digit moving to the right from the LSD, which stands for the "Last Significant Digit." The intermediate (partial) figures are stacked on top of each other, and then one digit is used to balance them out so that they match numbers with the same amount of significance. The whole product may be calculated by adding together all of the components that go into it. Even though the vast majority of participants only discuss multiplication in base 10, this relates to all bases, including binaries, in an equal manner. The progression of the data using the straightforward method described above is shown in Figure 1.1. A single person is represented by a single black dot.

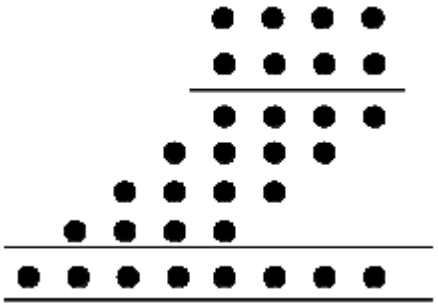

Figure 2.1: BASIC MULTIPLICATION

The most significant bit (MSB) is assumed to be the digit symbol there. The mechanism of multiplication is reasonably straightforward in relation to power systems. The parallel computer was responsible for computing this result for the two-number component. This approach makes use of the addition and move-left operations in order to derive the result based on the binary factors. In light of the approach outlined above, it is even possible to derive an algorithm for the various forms of multiplication. During this phase of the process, we are also able to test if the product is good or poor, as well as whether the MSB of the tests reveals the indication of the product once we have received the full result.

2.3 MULTIPLICATION PROCESS

Calculating a two-number element directly by hand is the most straightforward way to do an arithmetic operation. This process may be broken down into three steps: the first phase involves some development of the commodity, the second step involves some reduction of the commodity, and the third step involves some introduction of the finished product. Calculate a product via the hands of 2 using two more numbers, such as 11012 (310) and 01012 (510, "which may be described in figure 2.1 This will provide additional information on the operating procedure. Measure the thing by hand so you have a point of reference.

The numbers written in strong italics are the continuation of signals for the things that are not complete. The first codeword may be thought of as the generator, while the other can be thought of as the accelerator. The incomplete items are referred to as incomplete goods, whereas the completed product is considered to be the standard. Nevertheless, if

this process is directly applied to a piece of machinery, the resulting multiplication cycle looks like what's seen in the image. As can be seen from the figures, the creation of PP, the reduction of PP, and the completion of the subsequent stages are all examples of arithmetic operations in hardware. The two varieties are known as sum bits and communicate bits.

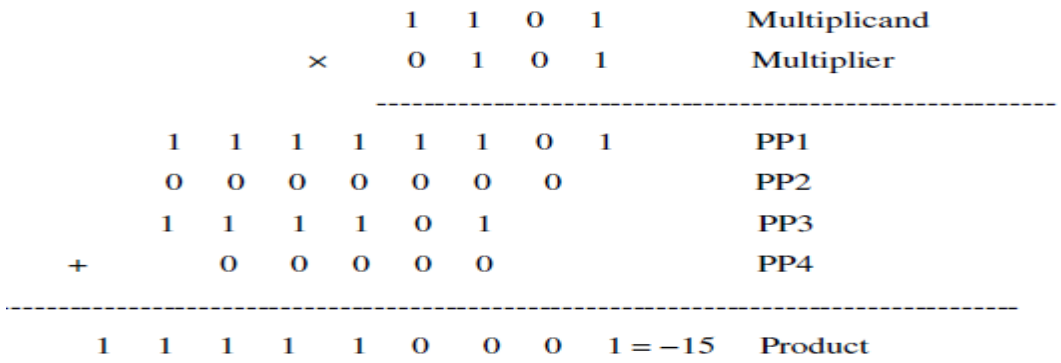

Figure 2.2 MULTIPLICATION PROCESS

This method involves moving one bit of multiplication across from side to side at a time, subtracting the multiplicand from the multiplier's single bit, and then moving the intermediate product one spot to the left of the earlier intermediates. This method is used to solve problems involving multiplication. Add together all of the individual components of the partial products produced by each column to obtain two parts: total and transport. In each column, both the total and the bits need to be put together. Similarly, one may generate a product that is n+m bits long and consists of m component products in order to do the computation for the n-bit multiplicand and the m-bit conversion.

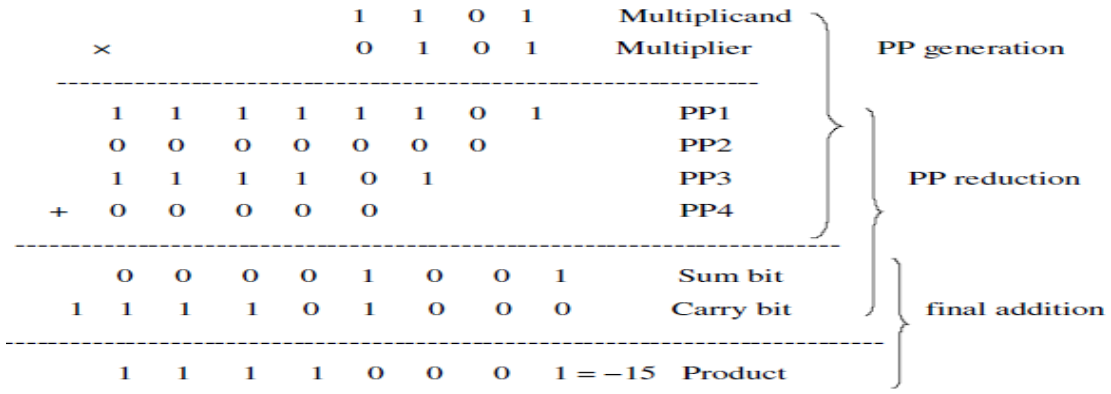

FIGURE 2.3 MULTIPLICATION, DISPLAYING BOTH THE TOTAL AND THE CARRY

This method involves moving one bit of multiplication across from side to side at a time, subtracting the multiplicand from the multiplier's single bit, and then moving the intermediate product one spot to the left of the earlier intermediates. This method is used to solve problems involving multiplication. Add together all of the individual components of the partial products produced by each column to obtain two parts: total and transport. In each column, both the total and the bits need to be put together. Similarly, one may generate a product that is n+m bits long and consists of m component products in order to do the computation for the n-bit multiplicand and the m-bit converter.

2.4 BINARY MULTIPLICATION

The set [0, 1] is the only one that may contain bits when using the binary digits approach. When each binary digit is multiplied by a single binary integer, the result is either 0 or the starting total. Because of this, the formation of partial intermediates may be accomplished quickly and efficiently. When it comes to binary multiplications, these incomplete items are the task that takes the most time. Forming the part-products one at a time and tallying their totals as they are generated is one method that makes logical sense. This technique is effective, but it is slow since it requires at least one computer cycle to count each extra part-product. This strategy is often implemented by software on computers that do not have a hardware generator. Although it is effective, this strategy is sluggish. It is possible to directly install multipliers into equipment in those systems where the efficiency offered by this method is insufficient. The signed and unsigned number groups are the two primary categories used in binary arithmetic. Digit multiplication is accomplished by performing a series of bit swaps and sets of bit additions, and the final result combines the two numbers that are being multiplied together. It is necessary to do unmarked multiplication using the multiplicand x = xn-1..... x1 x0 and the multiplier y = yn-1..... y1y0 in order to construct the component of up to n shifted multiplicand copies. It is composed of three stages: the initial development of a partial product, the reduction of a partial product, and the final addition.

2.5 DRUM (DYNAMIC UNBIASED MULTIPLIER)

The vast majority of programs used for data analysis, computer vision, and artificial intelligence exhibit a significant amount of tolerance for practical errors. This stability defect might be used to reduce accuracy in order to achieve savings in power consumption and architectural design. It expressly concentrates on the process of multiplication, which is an integral arithmetic operation for such applications, and presents a novel estimated multiplier with such a dynamic selection method. We design the multiplier to have an unbiased distribution of errors so that it can be used in fewer real-world applications of artificial intelligence. This is done despite the fact that the errors will cancel each other out rather than accumulate as the multiplier is used repeatedly for computations. The provisional architecture may also be customized, giving the designer the ability to deploy resources inside it according to the level of accuracy and power they need.

In addition, multiplier benefits from a reduction in propagation delay, which makes it possible for it to be used on the important route. Theoretically investigate the inaccuracy that arises from this design's variables, then put the design's output through the paces using image analysis and computer classification software. This demonstrates that its architecture is capable of achieving power savings of 54–80 percent while simultaneously introducing modest mistakes with a Gaussian distribution with a near-zero average and standard variations of 0.4–3.61 percent. In addition to this, it records power savings of up to 58% when the updated design is implemented. It suggests that this idea is more advanced than several estimated multipliers that have been recently proposed in the literature.

They introduce a novel Dynamic Range impartial Multiplier that may be used in situations that are approximative. The multiplier is able to "zoom in" on the numbers that are most relevant because to the dynamic nature of the architecture, which also makes the multiplication process more scalable and flexible. The availability of this multiplier, which is not biased in any way, helps to ensure that the average error is as close to zero as possible. Standard calculations need a very large number of multipliers. As a direct result of this, the objective method promotes mistakes that compensate for one another rather than adding up to a greater whole in the ultimate result of the measurement. Because of

the flexible nature of this design, it is possible to make a seamless trade-off between being academically dishonest and the amount of power used, depending on the priorities of the designer. In addition, an estimated version will make use of a key correct multiplier that is lower than the entire multiplier. Therefore, programmers are able to apply the key factor multiplier template of their choice without giving up the tasks associated with conventional design.

2.6 ARRAY MULTIPLIER

There is a significant amount of research interest in the development of layouts for high-speed, low-power, and regular multipliers. It is possible to adjust the multiplier rate by lowering the partial products. During an amplification process, there were many different efforts attempted to lessen the quantity of incomplete products that were generated. In order to summarize the products in the allotted amount of time, a half-adder array multiplier was used. VLSI circuit designers have a significant obstacle in the creation of high-speed circuit boards that use little electricity.

The vast majority of arithmetic operations are carried out by multipliers, which are the element in digital circuits that use the most power. The hardware community has a solid grasp of the multiplication cycle in terms of the move and add operations. The optimization of the adder was a contributor to the improvement of the multiplier's efficiency. A modified full adder that makes use of a multiplexer is proposed in this work as a means of achieving low multiplier power consumption.

For the purpose of assessing the performance of the design, the conventional multiplier array structure is being used. Verilog HDL is used to decide the design, while Xilinx is used to simulate the functionality of the design. The results of the ASIC synthesis of the suggested multiplier reveal that there is not a significant difference between the present techniques in terms of power use (35.45%), region (40.75%), or delay (15.65%).

Increasing the quantity of calculations that can be done by increasing efficiency is a more efficient way. To cut down on switching power dissipation by 22%, a multiplier that uses partial product encoding MBE and a method called spurious power suppression approach is recommended. The bits of a multiplication are shown going from high to low order as a result of transition frequency. The array multiplier is distinguished by having a linear

form. Attach and move is the foundation of the multiplier module's operation. One multiplier bit multiplication is used to create each and every one of the partial products. However, rather of being detached, the partial component is shifted to its bit ordering and connected. The conventional carry spread adder may be used in order to accomplish adding. If N has a multiplier length of 2.7, then N-1 adders are required.

2.7 BAUGH WOOLY MULTIPLIER

The act of multiplying two or more numbers together is a dynamic arithmetic procedure. The multiplication of processed signals is a basic operation, while multipliers have a large range, require a substantial amount of resources, and have a lengthy latency. Another component that is absolutely necessary for low-power VLSI device design is low-power multiplier architecture. The design of a parallel multiplier can typically be broken down into three distinct stages: the first stage involves the generation of bit partial products through the use of straightforward AND gates or through the implementation of various recoding methods; the second stage involves the compression of bit partial products through the implementation of either a standard or an unusual logarithmic tree array; and the third stage involves the extension of bit partial products.

The reduction tree approach, which was used in the creation of a new Baugh Wooley multiplier architectural design, is the primary component of this multiplication. The High-performance Multiplier (HPM) reduction tree relies heavily on partial product compression as its fundamental building block. It is quite normal, and the communication between the HPM inserting cells takes the shape of a triangle. The use of triangular forms may be justified due to the fact that the arrangement of triangular cells in the method of reduction trees results in a shorter wire length.

One of the effective methods for controlling symbol bots is known as Baugh-Wooley replication. This strategy was created in order to construct frequent multipliers for two-digit integers that compliment each other. Let's multiple the multiplier(A) and the multiplicand, which are both n-bit values (B). Both A and B may be represented by the following equation: A = an12 n1 + ai2 I n2 i=0 −bn−12 n−1 + bi2 I n−2 i=0

The outcome of the classic 8-bit Baugh Wooley and Modified Booth multiplier algorithm was in stark contrast to that of the contemporary 8-bit Baugh Wooley and Modified Booth predictor algorithm that made use of an HPM reduction tree. This was due to the architecture and implementation of each algorithm. Through the use of comparative study, it was determined that the contemporary Baugh Wooley converter idea is speedier than both the modern and HPM Changed Booth multiplier concept as well as the classic Baugh Wooley converter concept. The Hatamian scheme is the primary topic of this. It may be broken down into the following steps: 1) In the Baugh Wooley algorithm, the most significant bit (MSB) of each N-1 row and all bits of the final part-product row, with the exception of the MSB, are inverted. 2) In the Nth column, add the number 1. 3) The most significant bit, or MSB, is then inverted.

Using the HPM technique to implement the Baugh Wooley factor is basically a straightforward approach that is detailed in the methodology. The AND gates may be used to compute partial products, whereas the NAND gates can be used to create inverted products. Insertion of the number 1'. An area that uses the Baugh-Wooley method is one in which the operands either match or transcend 32 bits. In order to calculate direct percentage increases for Two's sum, the Baugh-Wooley approach was devised. When you combine the published additive numbers from Two, each partial component that you add together makes up a signed quantity. Therefore, in order for the Bring Save Adder to provide an accurate total, each partial product has to have its length increased to match that of the final product.

2.8 BOOTH MULTIPLIER

The technique used by Booth to remove level measurements is ingenious. The ability to connect and detach a component many times is required to commence this process. The Booth algorithm is a multiplication method that needs two additional signed binary values in order to do the multiplication. The process of duplication in earlier times often included a series consisting of addition, subtraction, and then shifting. The process of multiplication may be simplified to the process of making numerous additions. The quantity that has to be applied is referred to as the Australian indigenous, the number of

times that it needs to be input is referred to as the multiplier, and the total that we get is known as the multiplication product.

Following the phase of growing, a fraction of the product is produced. If the operands are integers, the output will often be twice as long as the numbers themselves in order to maintain the quality of the information. This method of doing repeated additions, which is indicated by the numerical description, is slow since it is often replaced with an algorithm that uses positional representation. There is a possibility that we may divide percentage rises into two halves. The first portion of the process is devoted to the development of a single product, while the second phase extracts, and then integrates, the information. The fundamental principle of multiplication may be broken down into two parts: the measurement of a partial product, and the analysis of a set of moving input signals. The execution of it is carried out by the consecutive column contributions of the relocated modified booth matrix.

The suggested multiplication method is really thorough. When doing addition via unmarked addition, it is not necessary to recognize the number sign. Although the same process cannot be used in signed multiplication because the signed integer is in a form known as 2's complement, which, if multiplied in a manner identical to unsigned multiplication, would result in the production of erroneous data. The sign indicating the final outcome is kept by Booth's algorithm. Multiplication, where strings of 0s in the multiplier make it possible to just move. When doing multiplication, operations need to be performed at each and every point. The multiplier contains strings of ones. At the spots on the multiplier where there is a turn from 0 to 1 or 1 to 0, all we need to do is just attach or subtract.

There are really twice as many pieces in our firm as there are operands to do. Add uf0' as the preceding LSB if this is the FIRST step in the sequence. The following are examples of possible arithmetic actions: 00:- shifting by itself is not sufficient to execute any mathematical operation. 01: Use the multiplier on fifty percent of the component on the left, then move. 10: First, remove the multiplicand from the component's left side, and then go to step 11. 11: no mathematical operation is carried out in this step.

2.9 Approximate Value of the Multiplier

A short description is given of some of the prior research on directly proportional to the concentration. Based on a device known as a broken-array multiplier, an approximation multiplier and adder have been proposed (BAM). By applying the BAM approximation approach to the standard adjusted booth multiplier, the estimated signed booth multiplier produced savings in energy consumption ranging from 28.6% to 58.6% and reductions in region ranging from 19.7% to 41.8% for various term lengths in comparison to a traditional booth multiplier that indicated an estimated multiplier. These savings were relative to an estimated booth multiplier.

An almost signed 32-bit multiplier that is used for prediction purposes in pipeline processors was optimized to be 20% faster than a full-adder-based leaf multiplier. This was accomplished while maintaining an error probability of around 14%. In an error-tolerant multiplier, which calculated the approximation result by dividing the multiplier into one accurate and one estimated component, the accuracies for varied data widths were stored. This allowed the error-tolerant multiplier to identify the result of the approximation. It was claimed that a 12-bit multiplier might reduce its power consumption by more than half. Designed and tested two approximated 4:2 compressors that may be used in a Dadda standard multiplier.

The literature discusses the use of approximated multipliers for computer vision applications since it leads to reduced power consumption, lower latency, and fewer transistors as compared to those with an accurate multiplier nature. It has been claimed that mistake-resilient systems use multiplier architecture, also known as ACMA. The ACMA employed a method known as carry-in prediction, which was based on a pre-computation logic, in order to improve the amount of output it generated. The estimated computation that was proposed resulted in around a fifty percent decrease in latency when compared to the real version. This was accomplished by increasing the important route. Estimated factor of reproduction for Wallace trees (AWTM). Carry-in estimate was used once, and it was employed to get to the important route. Throughout the entirety of this investigation, AWTM has been utilized in a real-time comparison picture test. The results of this test demonstrated power and region reductions of approximately 40 and 30

percent, respectively, with no degradation in image quality when compared to the utilization of a direct Wallace tree multiplier (WTM) framework.

A approximately unsigned multiplication that is reliant on the conditional operand logarithm is what is proposed here. The product of the operation that is proposed to be multiplied is determined by adding together the logarithms that have been calculated. After then, the multiplier concept is generalized to a change, which leads to the introduction of operations. Advised as part of a procedure intended to improve the accuracy of the multiplication method. The input operand decomposition was the primary emphasis of this method. This strategy resulted in a significant rise in the average number of failures while simultaneously driving up the expected multiplier hardware costs by almost twice as much.

A Dynamic Segment Method (DSM) is used to conduct multiplication on an m-bit segment beginning from the top one bit of the input operands. This method is shown as an example. A dynamic range unbiased multiplier, sometimes known as a DRUM multiplier, was developed. This multiplier chooses an m-bit portion of input operands, starting with the leading bit, and then changes the least important bit of truncated values to one. Within this methodology, the values that have been truncated are multiplied with the ones that have been left over. It has also been proposed that about 4 WTM may be obtained by employing an inaccurate metric of 4:2. In addition, a device for the identification of errors was suggested as a solution for fixing outputs. This shaky Wallace multiplier has the potential to be used in an array structure to produce multipliers with a higher factor.

Almost every one of the approximated multipliers that had been offered before concentrated either on modifying the structure of a specific exact multiplier or on making the task more challenging. In a similar vein, we recommend carrying out the estimated multiplication by reducing the complexity of the operation. The main difference between our study and is that, despite the fact that the fundamental ideas behind both studies are now almost similar for unsigned integers, the mean error in our recommended technique is much lower. When doing calculations using s square, we also suggest a few approximation strategies.

CHAPTER 3

LITERATURE SURVEY

A tutorial," written by M. Alioto IEEE Trans. Circuit: Recent deployments of wireless sensor networks, abbreviated as WSNs, are becoming more widespread. Their very existence is fraught with peril, and the ability to function is the single most significant limitation they face. The wireless sensor nodes, which serve as the network's central nervous system, are often powered by limited-capacity power storage devices (e.g. small batteries or supercaps). While listening inactively, wake-up radio signals may be an extremely beneficial tool. Because of this, several conceptual frameworks for wake-up radio receivers have been presented over the course of the last ten years. In this work, we present a sophisticated formulation and construction of a sophisticated wake-up radio that is capable of both processing the received data (i.e. address) and transmitting the data to the neighbors or, if necessary, waking up the message. This is accomplished through the use of a radio that can both wake up the message and transmit the data. These technologies have the potential to considerably increase the energy efficiency of communication while also enabling ultra-low power hop communications. The results of the experiments indicate that the proposed architecture, which is optimized for the development of energy-efficient and iterative MAC protocols in the future, is powerful and functional.

A low wattage is an absolutely necessary criterion for portable multimedia devices that use a variety of signal processing and architectural approaches. The vast majority of people will be able to glean useful information from relatively inaccurate outputs on multimedia apps. As a result, the results of the statistical analysis are not entirely accurate. Previous research has made use of the error's persistence, particularly via the process of voltage over-scaling, and has used architectural and computational strategies to reduce the number of mistakes. As an alternative way, we propose in this article that

the mathematical intricacy of the resistor be used to one's advantage in order to achieve higher levels of computing accuracy. In order to demonstrate that our approach is practical, we have constructed audio and visual compression structures by making use of the approximated arithmetical units that were recommended. Additionally, using these temporary adders, we are able to derive fundamental statistical equations about failure and energy consumption. In addition to this, we have shown the applicability of such approximated adders in two different optical signal processing frameworks, each of which have distinct efficiency requirements (discrete transforming cosines and finite pulse response philtres). Simulation studies demonstrate a power savings of up to 69 percent when the technology in question is used in combination with existing systems that make use of the appropriate adders.

H. Mahdiani, S. M. Fakhraie, A. Ahmadi, and C. R. Mahdiani. Lucas, "Bio-inspired inappropriate computational blocks for efficient VLSI software development," was published in the IEEE Trans journal. Tour: Tour.

In order to accurately measure the results of the computations that have been delegated, the standard machine blocks that include the different data network configurations are constructed. The most important aspect of the BICs that we have proposed is that they are not intended to provide an accurate value of the result but rather an acceptable estimate of the outcome at a lower quality. These more recent systems are more effective than their direct competitors in terms of both the playing field and the power they need. Within the scope of this study, we provide a comprehensive explanation of the BIC adders and multipliers construction samples, as well as the error behavior of each. These BIC structures may also be utilized to successfully deploy a neural network with three layers and the hardware fuzzified block of a fuzzy processor. Both of these can be accomplished via the usage of the BIC structures.

R. Venkatesan, A. Agarwal, K.Roy, and A.Raghunathan published the article "MACACO: modelling and investigation of estimated computational circuits" in the proceedings of the conference. Installation of information technology; computers; computer development; assistance with:

Over the course of the last few years, there has been a significant rise in the use of approximation computing in relation to a class of strategies. These strategies relieve the necessity for precise equivalence between the declared computation technique and the one that is being implemented. MACACO is the name of the structured technique that we suggest using for the modeling and analysis of circuits for different methods. Using measurements such as the worst-case error, average-case mistake, error likelihood, and error distribution, the suggested technique can be used to evaluate how well the rough circuit complies with traditional correct execution. This evaluation can be performed by comparing the worst-case error to the average-case mistake. The first step in the MACACO process is to construct a comparable extended test circuit that will represent the behavior of the circuit under a certain amount of stress over a predetermined amount of time. After that, we will construct a simulated error circuit, which will reflect the error for a certain input or response series on the estimated output of the circuit. In conclusion, we combine classic Boolean methods of Analysis (SAT solvers, BDD), in conjunction with computational methodologies, in order to assess the many metrics of importance to us (Monte-Carlo simulation). The approach that we have presented has been used to conduct an analysis on a variety of projected designs for blocks. Our research has shown that MACACO may provide a developer with the ability to systematically assess the impact of approximate circuits and choose the most appropriate approximate installation for their needs, which in turn encourages the use of approximate computing circuits.

The paper "New optical signal processing estimated multiplier," written by F. S. S. Abrishami and S. Farshchi M. Fakhraie may be found here.

Within the scope of this study, a low voltage multiplier is proposed. The technique of approximation known as Broken-Array Multiplier is used by the suggested multiplier in place of the conventionally modified multipliers. The entire multiplier's energy consumption is cut down by 58 percent using this method, while the manufacturing precision suffers as a result. The proposed multiplier is compared to other estimated multipliers with regard to the amount of power that it uses and its level of accuracy. A 30-tap low-pass FIR philtre has also been developed so that more testing may be done on the multiplier output that has been offered. Energy usage and accuracy are equivalent to that of the philtre standard stand multiplier when compared to this multiplier. The results of the test show that there was a reduction in power consumption of 17.1 percent with a corresponding decrease in performance SNR of just 0.4 dB.

"Power accuracy coping with an immature multiplier architecture," authored by Father Kulkarni, Father Gupta, and Father M. Ercegovac:

We propose an innovative design for a vector that makes use of the updated 2 to 2 incorrect construction block and has error functions that can be tuned. The correlation between our imperfect multipliers and correct multiplicative designs results in a power saving that ranges from 31.78% to 45.4%, with an average of 1.39%-3.32%. Through the use of image sorting and edge enhancement as model applications, we were able to demonstrate that our design achieves a 2X-8X improvement in Signal-to-Noise Ratio (SNR) while maintaining the same level of energy savings as compared to existing over-scale-based power error handling approaches. The power savings of multipliers in bigger models are designed by us, which highlights the fact that the gains are strongly dependent on the design. The power-quality compromise loop-centric technique is contrasted with the pure software solution, which relies on a JPEG illustration. In addition, we enhance the architecture such that the multiplier may be used in applications that are not error-resistant while still retaining the capability of using a retained adder.

D.R. Kelly, B.J. Phillips, and S.Al-Sarawi published a paper titled "Approx. signature binaryinteger multiplier for arithmetical data value speculation" in the proceedings of the installation of the architect architecture. The generation of the signal image:

The performance of the machine pipeline may be improved by speculating in the arithmetic operation on the basis of the early emergence of a predicted consequence. This is done so that the prediction of arithmetical data value can take place. Estimated multipliers can measure a product far more quickly than precise multipliers can, and the results of the approximate measurement are more likely to be accurate. In this work, the notion of an approximated multiplier family that may be employed in a hypothetical data channel is presented for the first time. In benchmarking applications, an error rate of less than 14% was discovered for a signed 32 TSMC Artisan 180 nm SAGE-XTM cell library multiplier that was synthesised by 32 TE32 Bit. This multiplier was found to be 20% quicker than the whole adder dependant multiplier tree.

K.Y.Kyav, W.L.Goh, and K.S.Yeo are examples of low-power high-speed multipliers. These multipliers are used in the development of error-tolerants in proc. IEE ext. IEE ext. Up. Up. Solid-state loops using electron devices:

In this article, a contemporary modeling paradigm is presented, and accuracy is discussed as a process parameter. By including accuracy as a design characteristic, which enhances the efficiency of both energy consumption and velocity, the bottleneck that now exists in the creation of contemporary digital ICs may be circumvented. The necessity for high-performance, continually expanding simple sequence components with low power consumption is what we want to meet.

The authors of built a 2-bit adder that is purposefully meant to be inaccurate in order to calculate the sum of the bits 1 and 2 of a binary value. This adder requires very little space, very little power, and a very short delay in the most basic form. Because it is easier to generate partial products using the radix-4 algorithm (also known as the adjusted Booth algorithm), a multiplier that uses this algorithm is very effective. In contrast, the radix-8 Booth multiplier is less effective because it is more difficult to generate odd products using this algorithm. After that, the approximation multipliers are related to the construction of a low-pass FIR filter, and they show that their execution is chosen over that of various inexact Booth multipliers. A high-speed and low-power implementation of a 3-bit flash analog to digital converter was shown in reference [16]. In this research, a thorough inquisition of a 3-bit flash ADC circuit that utilizes diode-based stacked power gating method and low leakage stacked power gating technique is suggested. The total number of techniques used is 18. These methods of power gating are quite effective in lowering both the standard power and the leakage current. In order to evaluate the power gating strategies, a simulation was carried out making use of the cadence virtuoso tool at the arranged power supply provided by the 90nm technology.

The authors of [17] suggested a method of fine-grained power gating, which involves positively and sequentially turning on or shutting off the power supply for functional components in advance. In the deep submicron technology, the power leakage has developed into a significant portion of the embedded processor's overall power usage [18]. According to the findings of the research, the method may reduce the dynamic power consumption of a LEON3 processor by 48% and the leaky power consumption by 39% while maintaining the same level of execution quality. The authors of [19] created a high-speed approach for the parallel augmentation of two binary values that were meant for the multiplication. This technique was built for parallel processing. It condenses their partial products into two rows, the sum of whose parts being identical to the product as a whole. Both approaches suggested a less complicated addition module as a way to cut down on the number of partial products. These studies presented multipliers that had a smaller area and an unique reduction plot, both of which led to fewer components and less interconnect overhead. All of the high-speed designs that take up a little amount of

space rely on Wallace or dada multipliers as their foundation. The authors of [20] suggest a MAC unit that is built using compressors as the building blocks. Truncated Adaptive Booth Multiplier (TABM) is the algorithm that they used to build the MAC in this. The 3:2 compressors equipped with a vedic 16-bit multiplier were responsible for the partial product reductions that were accomplished. The MAC unit was created using a pair of 16-bit vedic multipliers that operated in parallel, and the additional compression was achieved via the use of compressor-based 64-bit adders [21]. It was determined that both the total land area and the total number of LUTs were less when contrasted with their respective alternatives.

In the paper [22], the authors introduced a high speed approximate multipliers (HSAM) approach for low voltage circuits that used the least amount of current possible using the CMOS technology. These were implemented for a current feed operational amplifier, which is number 22, as well as the current conveyor. Within the area of mild inversion just below the threshold, the efficiency is at its highest [23]. Through the use of this technique, it is possible to concurrently expand both the gain and the bandwidth. According to the findings of the comparison, this way of CMOS design has the potential to decrease the size by about fifty percent of the smallest area that is now accessible. Gain is achieved regardless of the bandwidth being used. In the paper [24], the authors suggest a high-accuracy fixed with radix-16 booth multiplier (R16BM) and partial product generator. In this step, the partial products are changed in order to make the truncation mistake less severe. The PP alignment and error compensation network is responsible for achieving error distributions that are even throughout. For the purpose of compensating, a simple sorting network known as the scalable Montgomery modular multiplier [25] has been developed (SMMM). The sub division of the lower partial products section into minor and major products contributed to an increase in the compensation accuracies. Because the mean square error has been decreased and the power reduction factor has been increased, it is now appropriate for use in applications that include loss.

CHAPTER 4

EXISTING METHOD

4.1. INTRODUCTION

These probability approaches determine the chance of an element appearing in the truncated partial products of multipliers [11]-[16]. These methods have been provided as a way to cut down on the amount of time needed for simulations. Theoretical work in [11] led to the derivation of a circuit-generated constant compensation value, which was given the name probabilistic estimation bias (PEB). The generalized PEB (GPEB) technique was used in [12] to produce a more accurate prediction of the area penalty by incorporating information from additional columns (w) in the truncation section; the GPEB circuit offers an appropriate tradeoff between accuracy and area/power use. An adaptive conditional-probability estimator (ACPE) was proposed in [13] for use in compensated circuit design; the ACPE was proven to increase the accuracy of multipliers. [13] was cited as the originating source. The technique of compensation described in [14] and referred to as probability and computer simulation (PACS) coupled simulation with statistical methods in order to achieve high accuracy with a minimal area and time penalty. However, with these hybrid systems, the setting up of some components of the circuits takes a significant amount of time. The multilevel conditional-probability (MLCP) technique, in which conditional probability is handled in a more complicated manner, was selected for use in [15]. In spite of the fact that using MLCP makes it possible to attain a high level of precision, the area cost rises. On the other hand, using this approach, it is possible to achieve, on the basis of the column information (w = 3), a signal-to-noise ratio (SNR) that is comparable to the ideal SNR value of a post-truncated (P-T) FWBM. In this research, we provide a data scaling technology (DST) that has the potential to enhance the precision of all different kinds of low-error fuzzy world boundary models (FWBMs). The fundamental concept comes from a technique known as block floating point (BFP) [17]. The concept of scaling is used in this study, and each block of incoming data in BFP is assigned a joint scaling factor that is proportional to the data sample that has the greatest magnitude inside the block. The excess bits of the

multiplicand are used by the suggested DST in order to get low-error FWBM bits in a more effective and efficient manner. To be more explicit, the truncated partial products, which are used to estimate the compensation bias, are decreased thanks to this technique; on the other hand, the number of computations performed by the FWBM rises. In spite of this, the accuracy of the FWBM may be increased by including the DST circuit that has been suggested into it. According to the findings, implementing the suggested DST improves the accuracy of low-error FWBMs while adding just a little amount of space to the computational burden. The performance of the proposed DST-FWBM was shown using CMOS technology with a 0.18-micron feature size in a very large scale integration (VLSI) device. The DST approach that was presented was found to significantly increase the accuracy of all different forms of FWBMs, and as a result, it is appropriate for use in applications that call for a high level of precision, such as image processing.

4.2. LOW-ERROR FIXED-WIDTH BOOTH MULTIPLIER

In general, the 2L-bit product P can be expressed using a two's complement representation.

$$X = -x_{L-1}2^{L-1} + \sum_{i=0}^{L-2} x_i \cdot 2^i$$

$$Y = -y_{L-1}2^{L-1} + \sum_{i=0}^{L-2} y_i \cdot 2^i$$

$$P = X \times Y \qquad (1)$$

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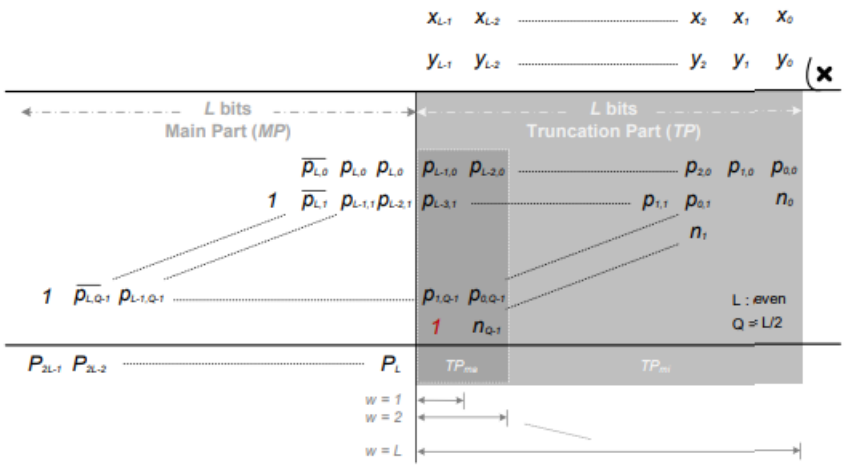


Fig. 1. Structure of FWBM

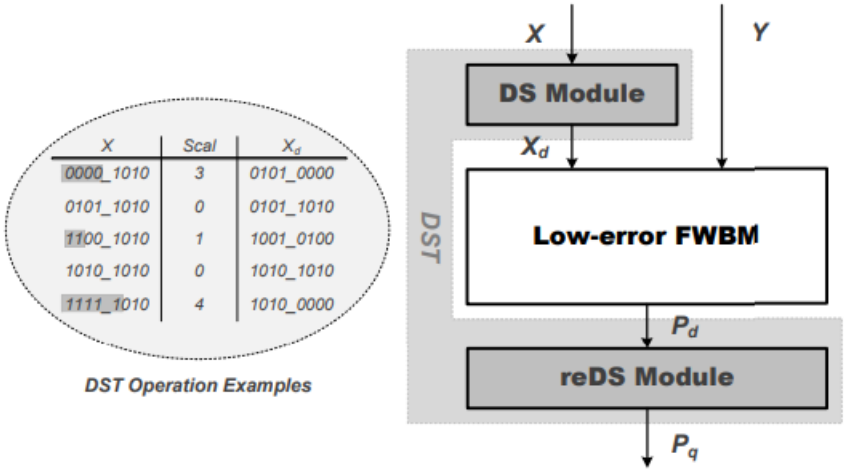


Fig. 2. Proposed DST used in low-error FWBMs.

FIG 4.1 STRUCTURE OF FWBM

FIG 4.2 PROPOSED DST USED IN LOW-ERROR FWBMS

4.3. DATA SCALING TECHNOLOGY

The DST approach that was presented is implemented into low-error FWBMs in the form of an extra circuit. Because of this, the circuit performance of the FWBMs is maintained, and the accuracy of the low-error FWBM is improved thanks to the DST circuit. When

doing DST, the superfluous bits of the multiplicand are used in order to acquire more information from the shortened T Pmi. The suggested DST for usage in low-error FWBMs may be found shown in Figure 4.2. Two different DST Modules are available (DS Module and reDS Module). One of them is placed above the FWBM with a narrow margin of error, while the other one is placed below the FWBM. The DS Module will move the Scal bit so that it corresponds with the redundant bit of the multiplicand X. The reDS Module will then rebuild the results so that they correspond with the corrected weight. The functions of the DS Module and the reDS Module may be expressed by the following equations:

Xd = X << Scal (5) Pq = ⌊Pd >> Scal (6), where Scal denotes the amount of bits that need to be moved in order to get rid of the unnecessary multiplicand X. If, for instance, L equals 8, X equals 8' b0000 1010, and Scale is 3, then Xd equals 8' b01010000. Additional instances of DST operations are shown in Figure 4.2. The values of Scale are determined by counting how many superfluous bits are found in the most significant bits of the multiplicand X. In most cases, the range of Scal is between 0 and L minus 1. A high value of Scal does, however, need a large number of bits to be shifted, which suggests that both a higher number of computations and a larger circuit size will be required. Thus, a limited shift bits (DSb) factor is introduced to limit the value of Scal; however, this would also limit the extent to which the accuracy of the FWBMs can be improved. Thus, there is a tradeoff between accuracy and circuit area. The SNR is used to analyze the effect of DSb on accuracy.

V. DST-FWBM CIRCUIT

the complexity and circuit area depend on the DSb. Thus, in this study, the tradeoff between accuracy and area cost was considered. As shown in Fig. 2, the proposed DS Module can be implemented using L D-to-1 multiplexers (MUXs) in which D equals (DSb + 1), and the reDS Module is designed using (L − 1) D-to-1 MUXs. Thus, the proposed DST circuit uses (2L − 1) D-to-1 MUXs, and the area of the entire DST-FWBM circuit is the sum of the area of the low-error FWBM and the (2L − 1) D-to-1 MUXs. To evaluate the area overhead and accuracy, the area of a 3- to-1 MUX is assumed to be twice that of a 2-to-1 MUX, the area of a 4-to-1 MUX is assumed to be

thrice that of a 2-to-1 MUX, and so forth. Thus, a (D − 1)-fold increase in area is required for a D-to-1 MUX over a 2-to-1 MUX.

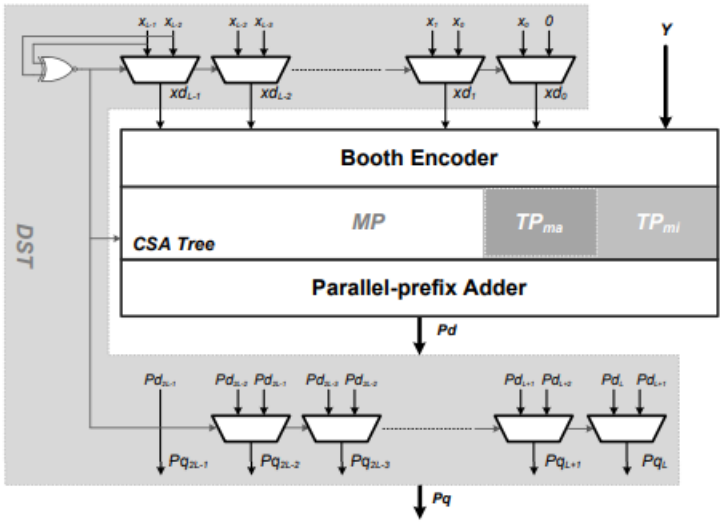


FIGURE 4.3. ARCHITECTURE OF PROPOSED DST-FWBM WITH DSB = 1.

The DSb value is multiplied by the region that would be affected by the proposed DST change. The examination of the growth in SNR, which is provided in Table, shows that the SNR does not continue to improve considerably when multiplied by the DSb value, and there is a noticeable improvement gap between DSb = 0 and DSb = 1 in the data. As a result, for the purpose of this investigation, we decided to set DSb equal to one since this number offers the greatest possible savings in terms of the suggested DST. Figure 4.3 depicts the overall layout of the DST-FWBM circuit that is being considered for use. On the other hand, when the suggested DST is utilized, the DSb value goes up, and the SNR value ends up being rather high. A DST circuit and a low-error FWBM are the two components that make up the proposed DST-FWBM, as shown in Fig. 4.3. The low-error FWBM might be a GPEB FWBM, an ACPE FWBM, a PACS FWBM, or an MLCP FWBM. The DST circuit is realized with the use of (2L1) 2-to-1 MUXs when textttDSb is set to 1. The FWBM is included inside the DST circuit and is made up of a parallel prefix adder, a carry-save adder (CSA) tree, and a Booth encoder. In every one of the FWBMs with a low error rate that was evaluated, the partial products from the MP, T Pma, and the predicted T Pmi are added together by the CSA, which may be made up of

either full adders or half adders. In conclusion, the high-speed parallel prefix adder is responsible for calculating the products Pd, and the DST circuit is responsible for obtaining the final results Pq.

CHAPTER 5

PROPOSED METHOD

5.1. INTRODUCTION

In the present climate, everyone is dealing with electronic equipment that include bulky circuits in some form or another, such as the many gadgets, computers, televisions, cameras, and so on. The realm of electronics has now grown into all sectors of modern life, including healthcare, medical diagnostics, vehicles, and other domains. It has taken a predicament and managed to persuade everyone that it is not possible to function without the use of technology. Logic gates are the elemental building blocks of a circuit since they are the only kind of electrical circuit that may be utilized to form any combinational circuit. The boolean logic underpins the operation of these combinational circuits. One or more switches that may be electrically controlled, such as transistors, come together to form a logic gate.

Another kind of multiplier is known as a programmable logic device (PLD), and it is built using look-up table (LUT) components. In order to calculate logical or arithmetic values, the LUTs may be programmed to function in the same way as any other logic circuit. This operates with values that have been pre-loaded from a specific place in memory. This makes it possible to simply reprogramme the circuit or correct a mistake without having to change the way the wires are arranged on the inside. These programmable logic devices are the ones that are recommended to use for outputs with a low volume. Over the course of the last several decades, there has been a remarkable evolution in the design of electronic multipliers. The first multipliers were created using vacuum tubes and transistors in their construction. The development of integrated circuits, in which all of the necessary logic gates were included on a single chip. Small Scale Integration chips were used for the first integrated circuits (ICs) ever created. In some cases, the gate count was just a very tiny number. The development of new technologies has enabled designers to fit hundreds of gates onto a single chip, leading to the creation of what are now known as medium scale integration chips.

The technology advanced to the point where it could now integrate on a broad scale and was capable of accommodating thousands of gates. The development of very large scale integration (VLSI) made it possible for the design of circuits on this chip to include more than a thousand thousand transistors. The capacity to include an N-thousandth of a given component's transistors is the measure of its complexity. The specific integrated circuit's (IC) level of complexity grows proportionally with the number of transistors that need to be built inside it. A larger number of the circuit's fundamental components would need to be used in its construction if it were a large circuit with several processing steps. In the present situation, the integrated circuits (ICs) are supposed to be constructed in such a manner that they might take less space, which would almost surely result in lower levels of power consumption. A very large-scale integrated circuit (VLSI) would only be considered efficient if it could use fewer transistors, shorten the time it takes for signals to propagate, and waste less power. When the circuit's complexity is reduced, it will undoubtedly be able to include a bigger circuit within the confines of the allotted space on the die of an integrated circuit. Therefore, it is possible to achieve compactness, dependability owing to a reduced number of interconnections, and lower power consumption. Because of the intricacy of the circuits, it is no longer feasible to verify the multipliers manually using the breadboards. At this point in time, electronic design automation tools were developed specifically for the aforementioned procedures. The verification process and the development of the layout also required the use of certain computer-aided methods. The inventors of the system constructed the gate level multipliers by hand until the total number of gates was significantly reduced. For the verification and design of VLSI multipliers, computer-aided methods become an absolutely necessary component. This also became popular for the automated placement of components and the circuit layout routing. It was necessary to evaluate the functioning of these circuits before they were built on chip, hence the development of logic simulators was necessary. Due to the increased complexity of the design, logic simulation was given a significant part to play in the design process [14]. The designers were able to address the functional problems in the architecture and sort out the defects, if any, in the

design before it was built. Before it was fabricated, the designers sorted out the flaws in the design. The major contributions of this work are as follows:

- Design and implementation of DST-R4BM, which can perform the high-speed variable width multiplication operations.
- Implementation of radix-4 modified booth encoding for optimized partial products generation.
- Implementation of DST, which can perform the recoding adder in parallel manner with reduced stages.

5.2. PROPOSED MODEL

The multiplication of two operands consists of a few steps, including the ones that have been described: recoding, multiplication, reduction of the partial product, and final addition. The efforts that have been made to simplify and speed up the multiplication process have primarily focused on simplifying the recoding step and speeding up the reduction of the partial product. The different recoding procedures will result in a different number of incomplete products being produced. During the recoding process, the binary digits are converted into a signed digit that has as little unnecessary information as possible. If the radix has a greater value, the recoding of the operands might result in the generation of fewer partial products. The level of complexity and the amount of time required for processing are both reduced as a result of this. The value of the r in a radix-4 binary multiplication is given by the equation r=2m, where m refers to the number of bits that have been gathered together for the recoding. The operand is broken up into m bits, and the non-redundant radix digits are recoded as (-r/2,....-1,0,1,.....r/2) in order to fit into the space available. When doing a radix–r multiplication with a 'n' bit operand, the partial products that are formed for unsigned integers are (n+1)/m, but the partial products that are generated for signed numbers are n/m.

Higher radix signed recoding is not often favoured since the production of the partial product requires odd multiplications, which cannot be accomplished by simple shift operations due to the fact that these operations need an extra addition or subtraction. In spite of this, the most significant benefit of having a greater radix is that it significantly cuts down on the number of incomplete products that are formed. This work includes the

implementation of radix-4 multipliers, which, when applied to an n-bit operand, produce only n4 products (according to the equation nm), as seen below.

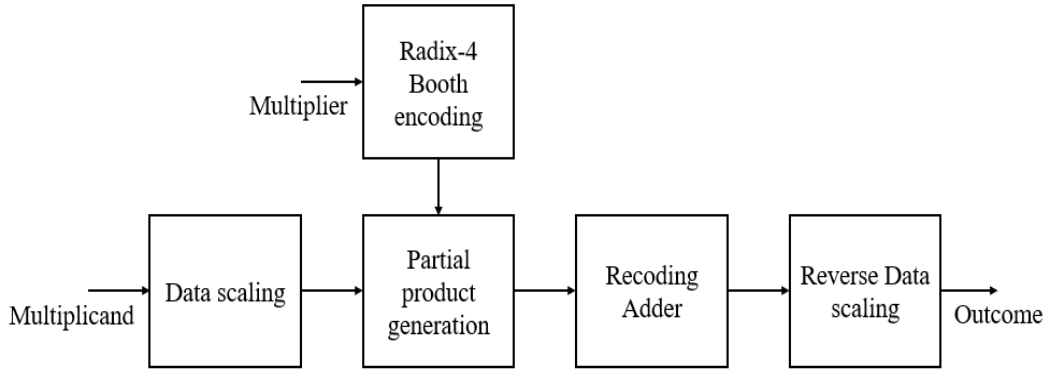


FIGURE 5.1. BLOCK DIAGRAM OF PROPOSED DST-R4BM.

The planned DST-R4BM is shown in the block diagram seen in figure 5.1. In this case, the inputs consist of an n-bit multiplicand (Y i) and a multiplier (X i), both of which have a bit content that ranges from 0 to n-1. The bits in the multiplicand are used to recode the operands, and each operand is recoded with a group of four bits from the multiplicand. An intermediate digit called w i and a transfer digit called t i are responsible for producing the recoded digit Z i for the collection of bits. The DST operation is implemented so that the recoding process may be carried out. In conclusion, the DST process produces the Z i in the following format:

$$Z_i = t_i + w_i \qquad (1)$$

The recoding is carried out in accordance with the values of the subset of bits that are clustered together. The value of the four-bit variable V i is used to determine how the values of the transfer and intermediate digits in the procedure are allocated. When the value of V i is less than 4, the transfer digit is zero, and the intermediate digit is assigned with the subset value V i. When the value of V i is more than or equal to 4, an alarm is sent with the value of V i being represented as V i = 8- (8 - Vi). In this stage, the transfer digit is created to the next place of the Radix-4, which is indicated by the notation (t i+1), and the intermediate value is recalculated to be equal to -(4- V i). This may be shown by

$$0 \le V_i < 2: t_i + 1 = 0,\ W_i = V_i,\ W_i\ \varepsilon\ [0, to\ 3] \qquad (2)$$

$$2 \le V_i < 4: ti + 1 = 1, Wi = -(4 - Vi), Wi\varepsilon\,[-3, to - 1] \qquad (3)$$

Due to the inclusion of the intermediate and transfer digits, the recoded final digit set now has the value "2,1,0,1,2." This can be seen in Table 5.1.

TABLE 5.1. PARTIAL PRODUCT REDUCTION.

X_i	Output	Operation
000	0	0
001	1. y_i	Multiplicand
010	1. y_i	Multiplicand
011	2. y_i	Left shifted Multiplicand
100	-2. y_i	Left shifted Multiplicand with twos compliment
101	-1. y_i	Twos compliment of multiplicand
110	-1. y_i	Twos compliment of multiplicand
111	0	0

The transfer digit is either a zero or a one, and this corresponds to the most significant bit (MSB) in the subset of four bits. This establishes whether the radix-4 digit is less than 2 or larger than 2. The very last thing that has to be done is to make sure that the transfer digit and the intermediate digit are placed to the right of the radix-4-digit position. In the case of an unsigned operand, the number of resulting recoded digits is equal to (n+1)/4, whereas in the case of a signed integer, it is equal to (n/4). When multiplying by 16 bits, the length of the recoded partial product is 4, whereas when multiplying by 64 bits, it is 16. After the recoding process is finished, the partial products are created by performing a multiplication of the multiplicand by using the recoded digits.

The computation of the multiplication of the digits with the multiplicand is done using a simple logical shift, with the exception of odd multiplies. The 1X do not need any operations, while the 2X are shifted logically by 2 bits correspondingly. The two's complement of the partial product at the bit location corresponding to the negative digit multiplications is used to arrive at the correct answer. The recoded digit may be obtained by using a total of three bits in this case, with the first bit having a zero bit attached to the right of it. The third bit comes from the set that is next to the current set. The result is a

code that may be multiplied by the multiplier in order to get partial products. A MUX is used to build a simple multiply and select unit. This MUX is put into the circuitry to produce the multiplied values, which range from one to two times their original value. The code generating unit is responsible for making the decision of which of the MUX's outputs to take. The previous result is used to get the inverted values for the negative multiplications, and then those values are transformed to their twos complement form. The expansion of the sign is required in order to do the signed multiplication, which takes up more room and territory. The concatenation of only a few bits is done for the whole row in order to make this operation more straightforward. With the help of recoding adders, the reduction of the so-called created partial products was brought down to two rows. After that, the partial products are combined together using the carry propagation array method, which results in the final multiplier conclusion.

5.3 CODE ADDER FOR RECODING

As was just said, Booth multipliers recode the operands so as to yield a small number of partial products. This allows the circuit to use less power and take up less space. Lower order radix multiplications are used extensively due to the fact that their execution is straightforward and they accomplish a sizeable decrease in the length of the partial product. The recoding of the multiplicand is accomplished by multiplying the radix digit that is formed as a result of the subset of bits that are taken into consideration during the operation of the multiplier. The value of the Radix-r multiplier determines the range of possible outcomes for the multiplication factor of the multiplier Y, which may range from negative to positive. The radix digits for multiplication are low for smaller radix multipliers, making it easy to multiply them using simple shift operations. At larger r values, the radix digit takes on values that cannot be multiplied directly by shift operations. These values prevent the radix digit from being used in calculations. They need to conduct some additions before they can complete the multiplication. In most cases, a CSA is used for the process of adding the intermediate multiples in order to arrive at the desired output.

The value of the radix digit for a Radix-4 Multiplier may range from -2 to +2. The even numbers just need a simple shift, whilst the odd values require nothing more than the

original value. In order to get the final number, the multiplication with odd digits requires a shift followed by an addition. The multiplication of the multiplier by the negative radix digit requires just an inversion in the result, which means that the value that was multiplied is the 2's complement of the original value. The recoding step is an integral part of the multiplier, and its contribution to the overall efficiency of the multiplier is significant. In order to improve the multiplier, the recoding step has to be quick enough to create products while still being an efficient user of energy. A specialized adder known as an approximation recoding adder is used to perform the operation of adding the data during the recoding step. This adder is sufficiently quick and releases less energy than its counterparts. In addition, the recoding adder is created using the parallel prefix of the ordinary CLA.

The sequential technique of PP reduction is easy to understand and follows a predictable pattern in terms of how the final product is formed. A modified approach of CLA configurations is carried out in order to cut down on the critical path as a means of overcoming the drawbacks of this structure. CLA configurations are organized in a hierarchical structure. During the first step, each PPR is added concurrently with the others. Therefore, at the first stage of addition, for a 16-bit multiplier that has 16 rows, there should be eight CLAs, each of which should have a length of 15 bits.

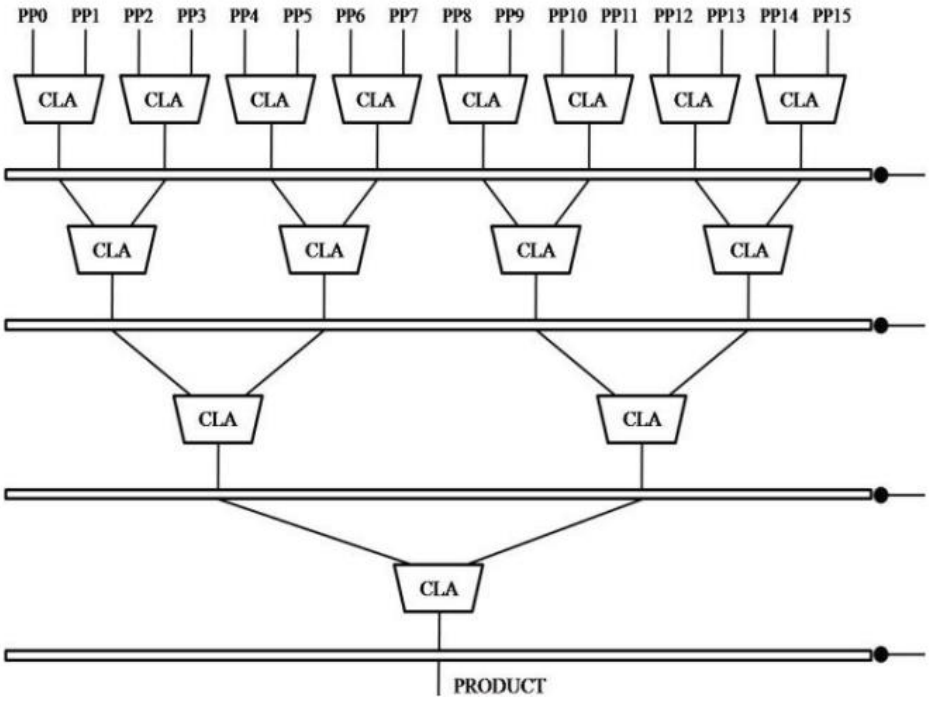


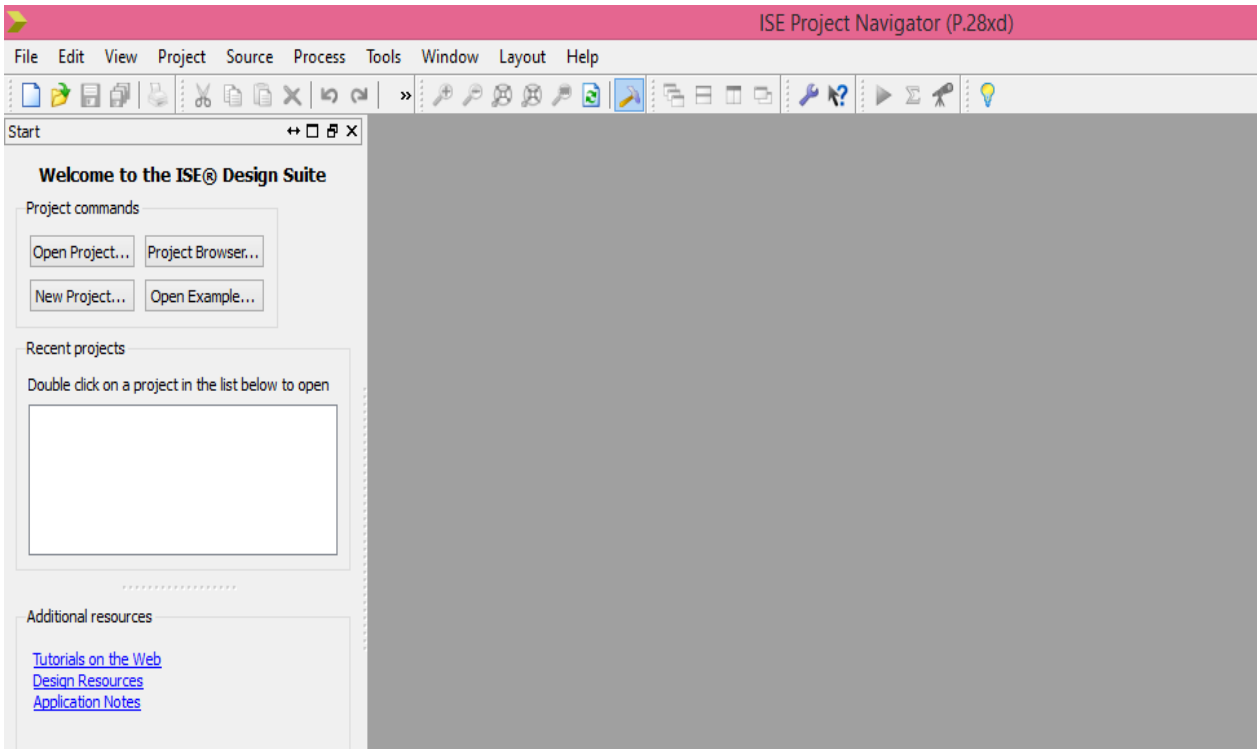
FIGURE 5.2. HIERARCHICAL STRUCTURE USED FOR ADDITION OF PPRS USING RECODING ADDER.

The two rows that are next to each other are put together, and then the results are created for the rows that are still available in the PP matrix. As a result, the system has eight rows of results, each of which corresponds to a carry. The last step involves combining these newly created results with four fewer CLAs, which brings the total to half its previous size. The addition of the result from the second stage, which results in two rows of data, in the third stage only requires two CLA to be completed. The addition of the result from the step above requires just one CLA to be performed in the final stage. This step is responsible for the generation of the final product of the multiplier.

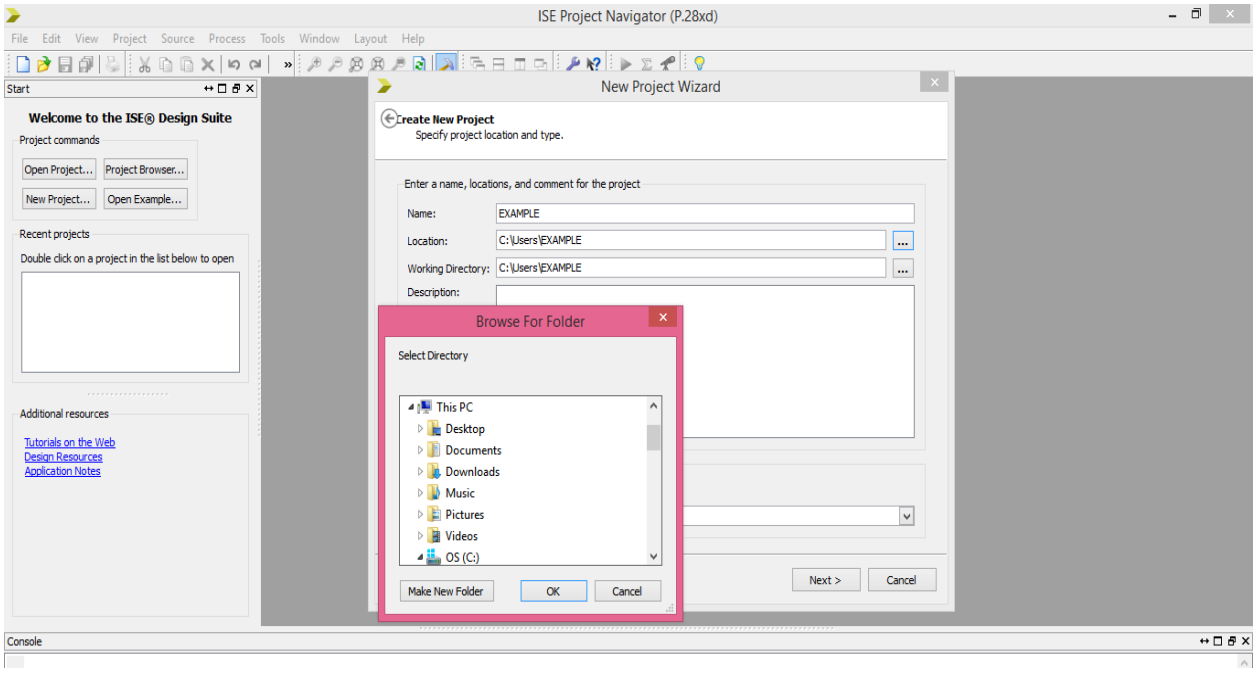
CHAPTER 6

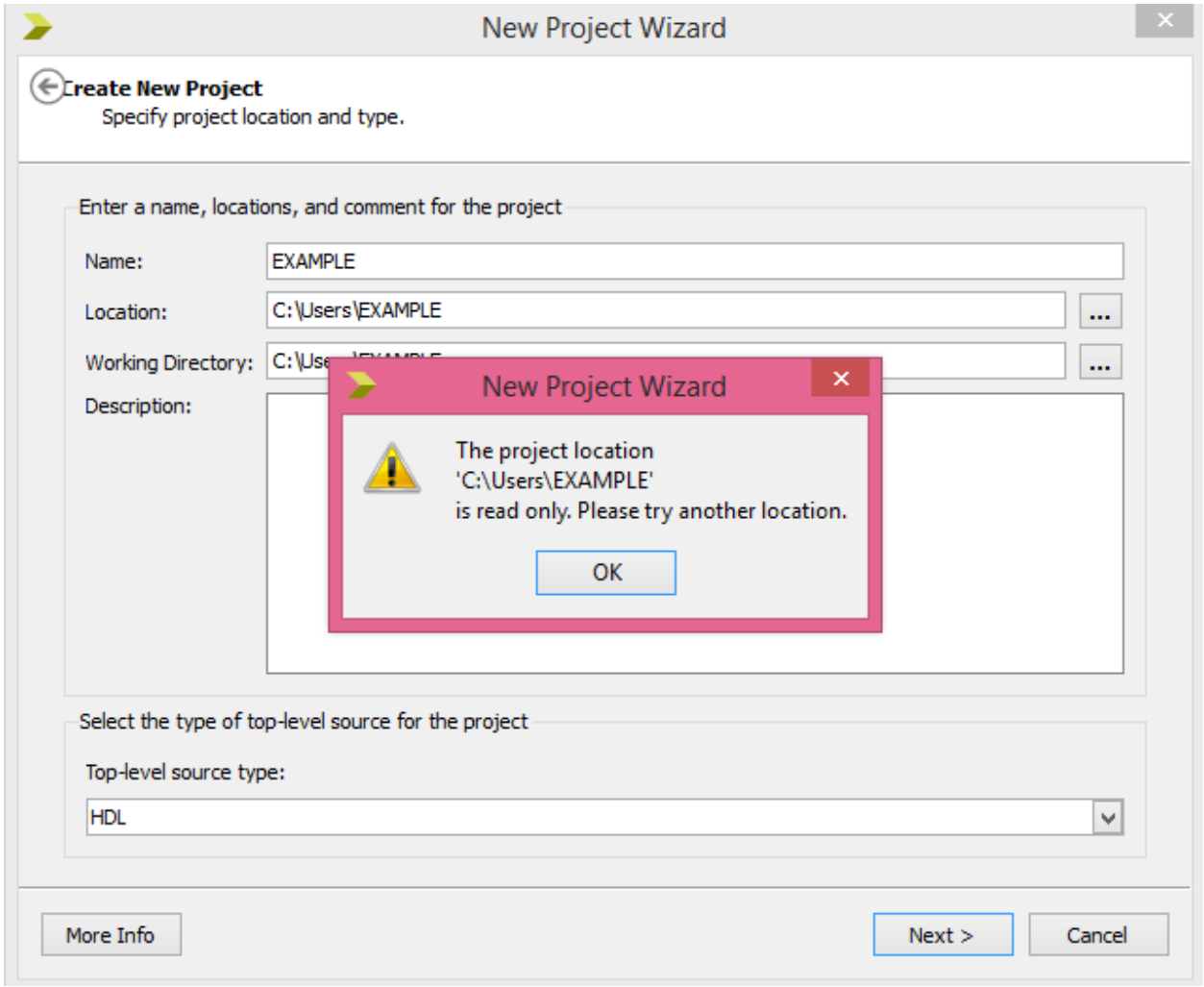
XILINX-ISE

Step 1: CLICK ON NEW PROJECT

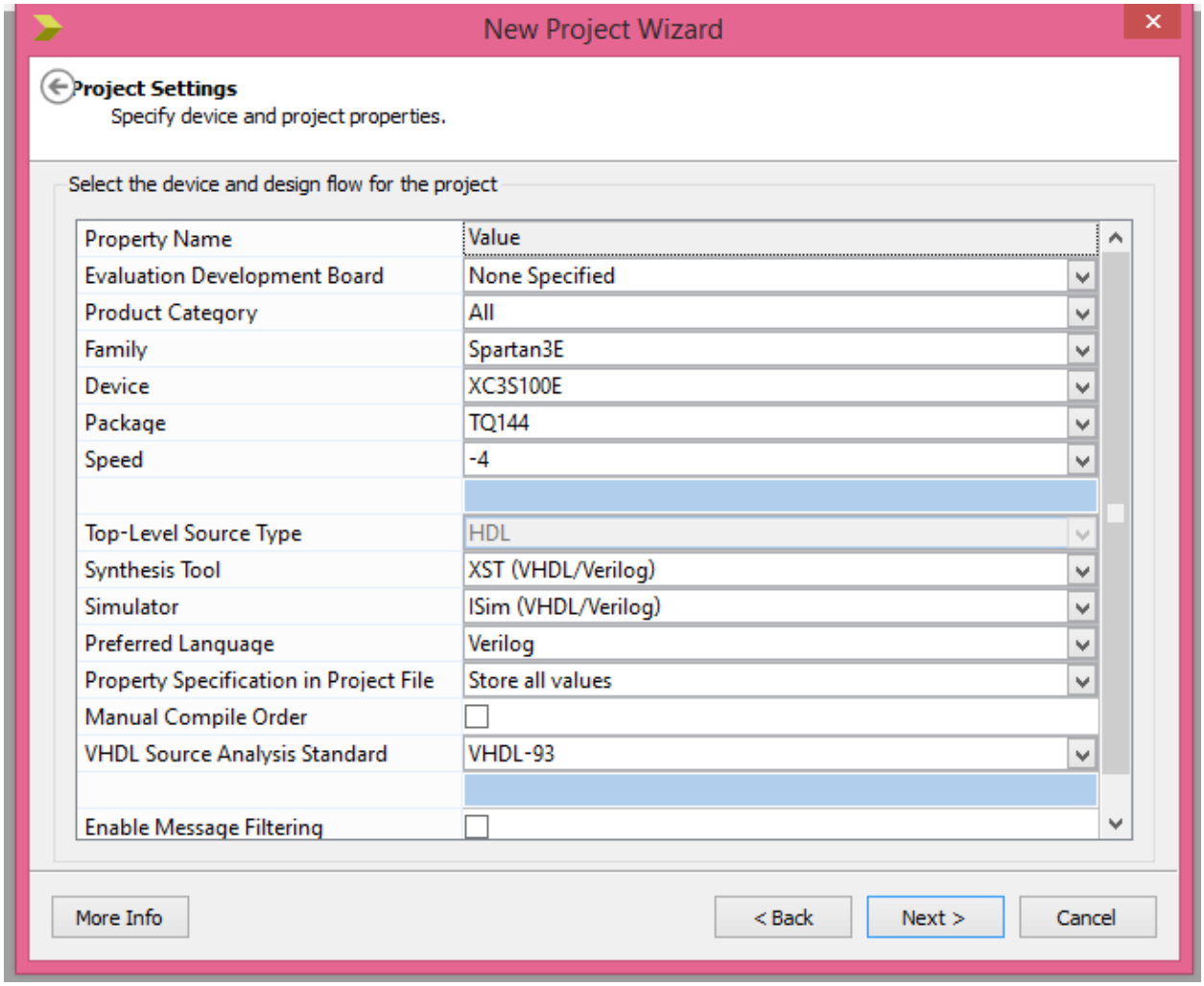


Step 2: GIVE THE PROJECT NAME and SELECT LOCATION (WRITABLE)

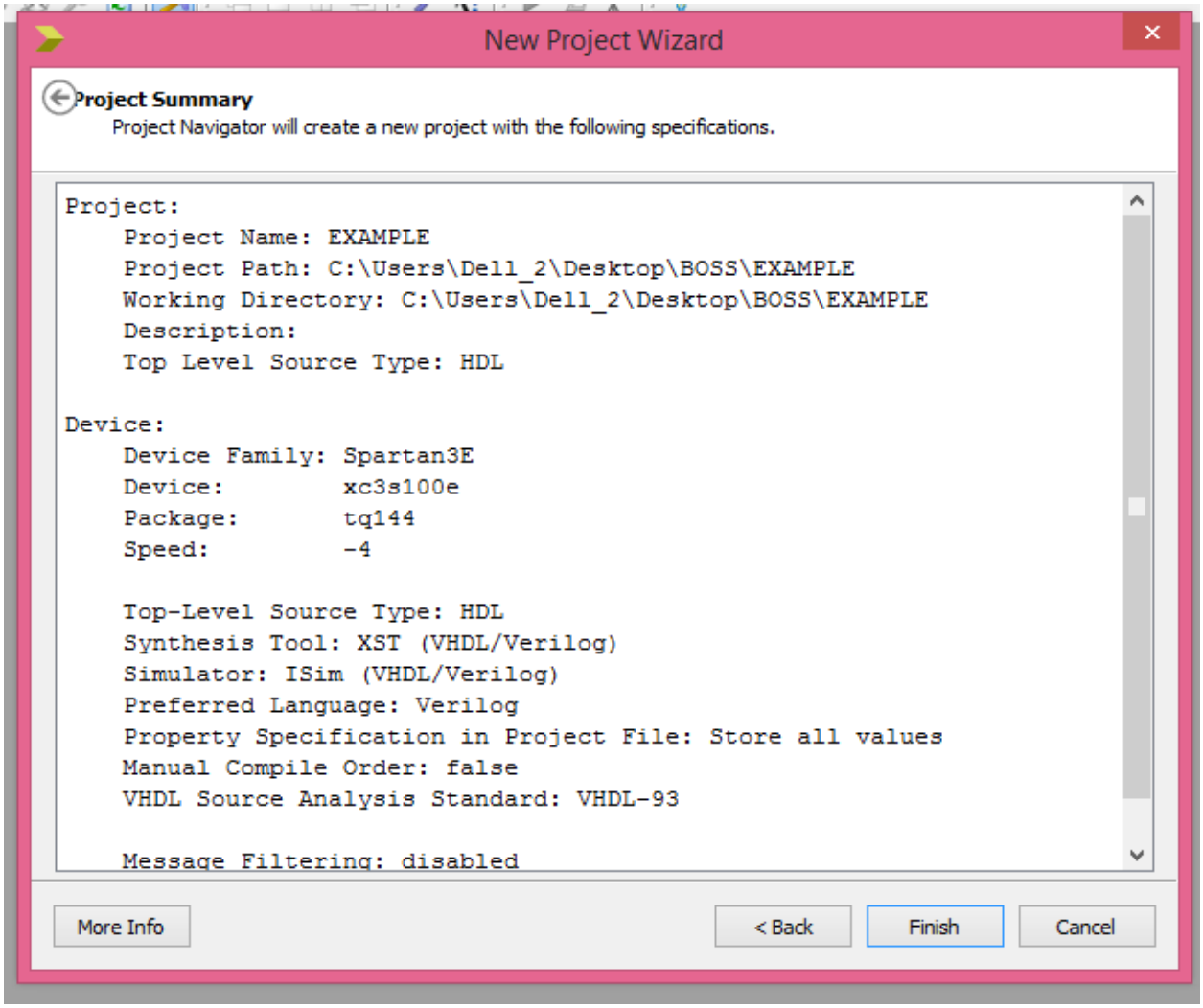

ISE Project Navigator (P.28xd)
File Edit View Project Source Process Tools Window Layout Help
Start
Welcome to the ISE® Design Suite
Project commands
Open Project...
Project Browser...
New Project...
Open Example...
Recent projects
Double click on a project in the list below to open
Additional resources
Tutorials on the Web
Design Resources
Application Notes
New Project Wizard
Create New Project
Specify project location and type.
Enter a name, locations, and comment for the project
Name: EXAMPLE
Location: C:\Users\EXAMPLE
Working Directory: C:\Users\EXAMPLE
Description:
Browse For Folder
Select Directory
This PC
Desktop
Documents
Downloads
Music
Pictures
Videos
OS (C:)
Make New Folder
OK
Cancel
Next >
Cancel
Console



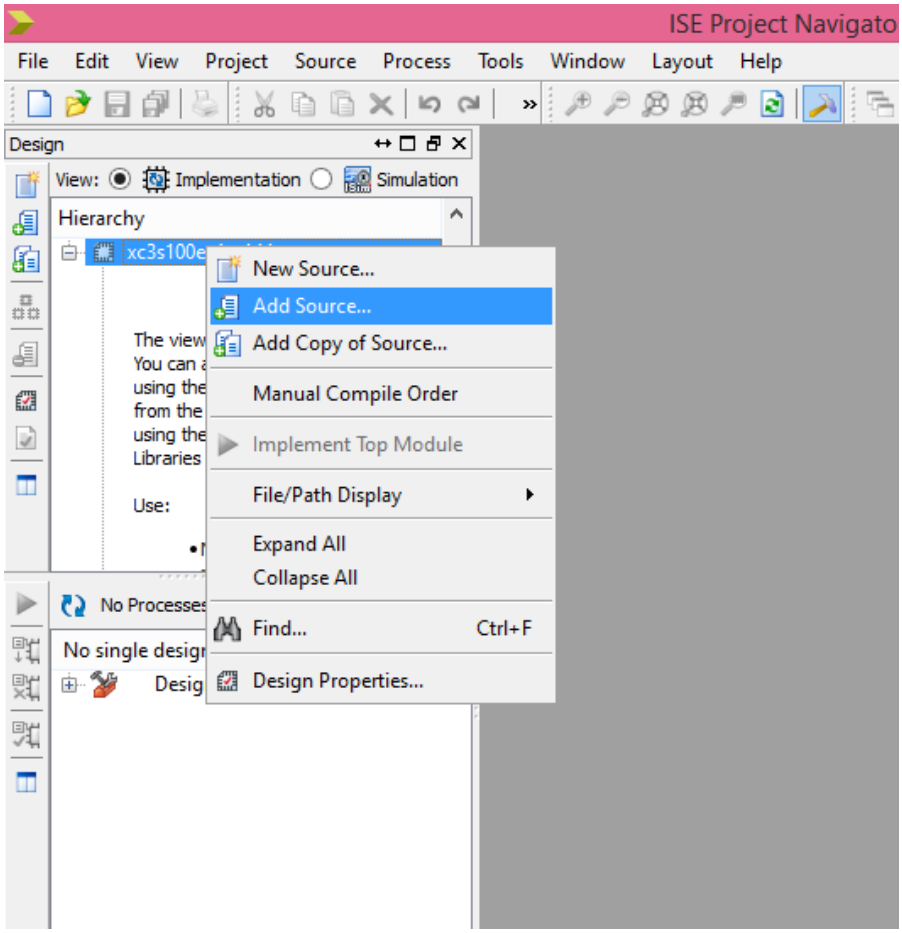
Step 3: CLICK ON NEXT and NEXT



Step 4: CLICK ON FINISH

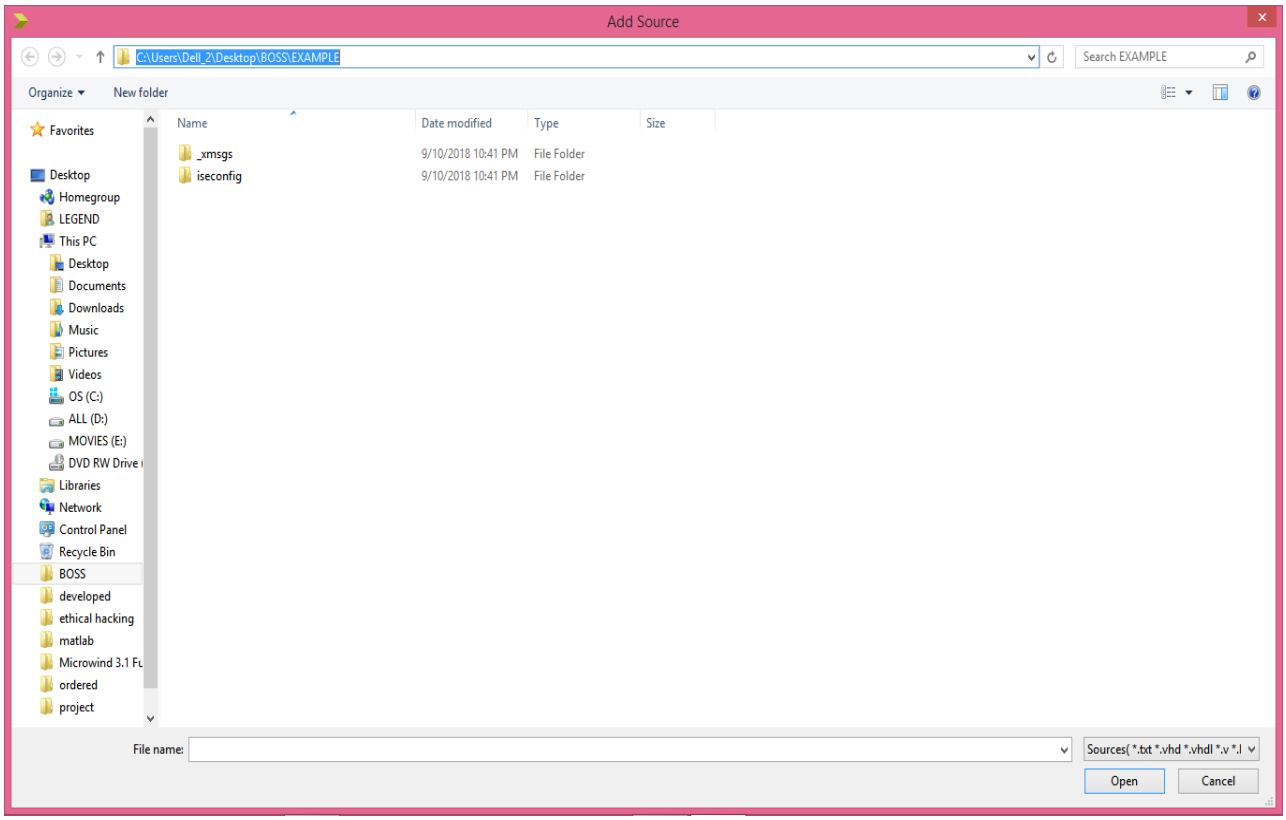


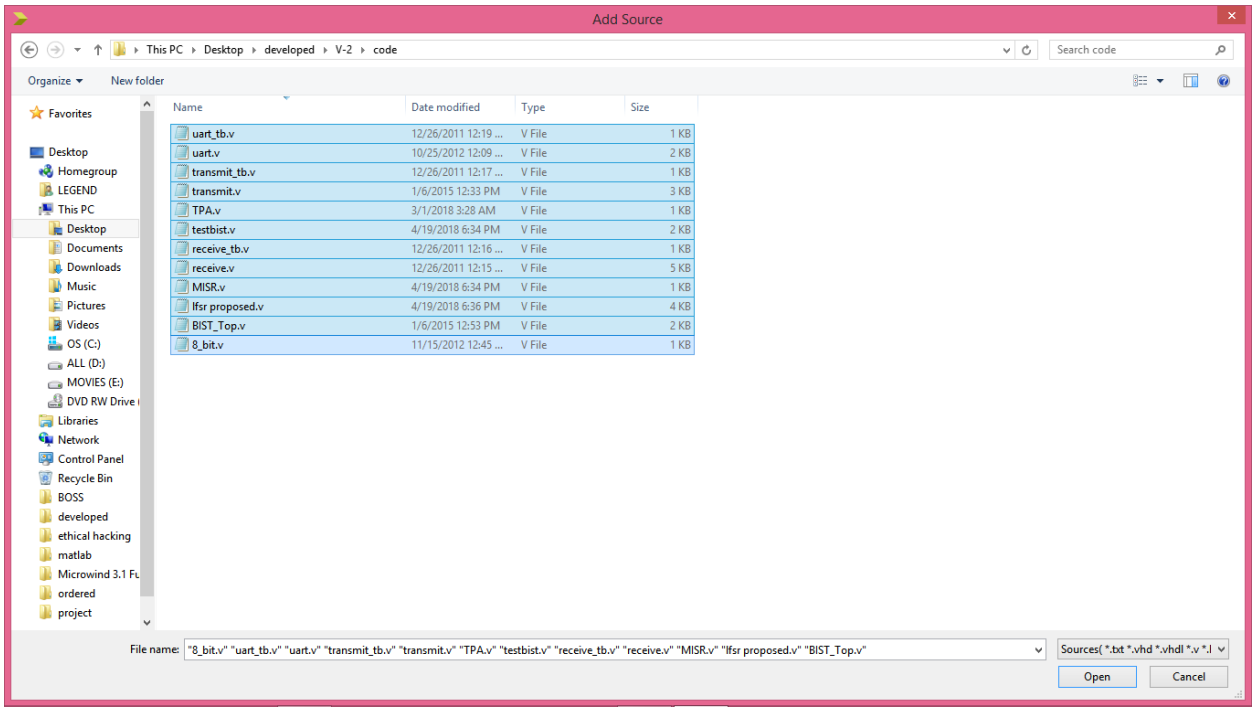
Step 5: CLICK ON CHIP (XC…) then MOUSE RIGHT CLICK then CLICK ON ADD SOURCE



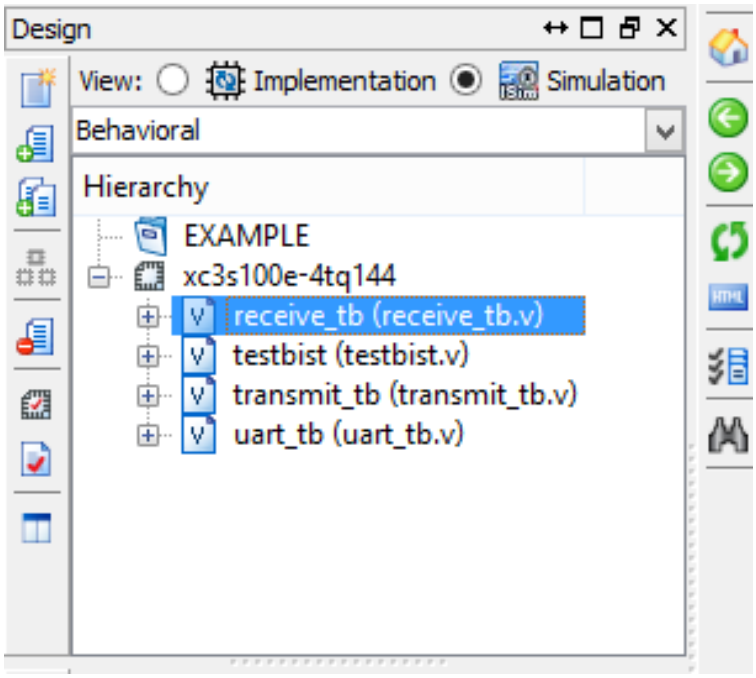
Step 6: SELECT THE CODE LOCATION GIVEN BY DEVELOPER AND ADD CODE

(Note ALL FILES) AND CLICK OPEN



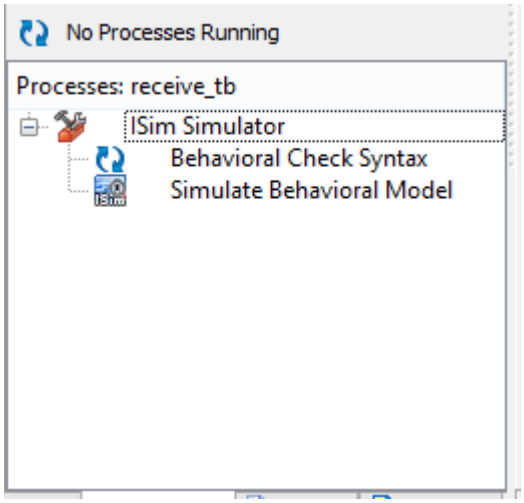


Step 7: SELECT THE SIMULATION and select files to RUN



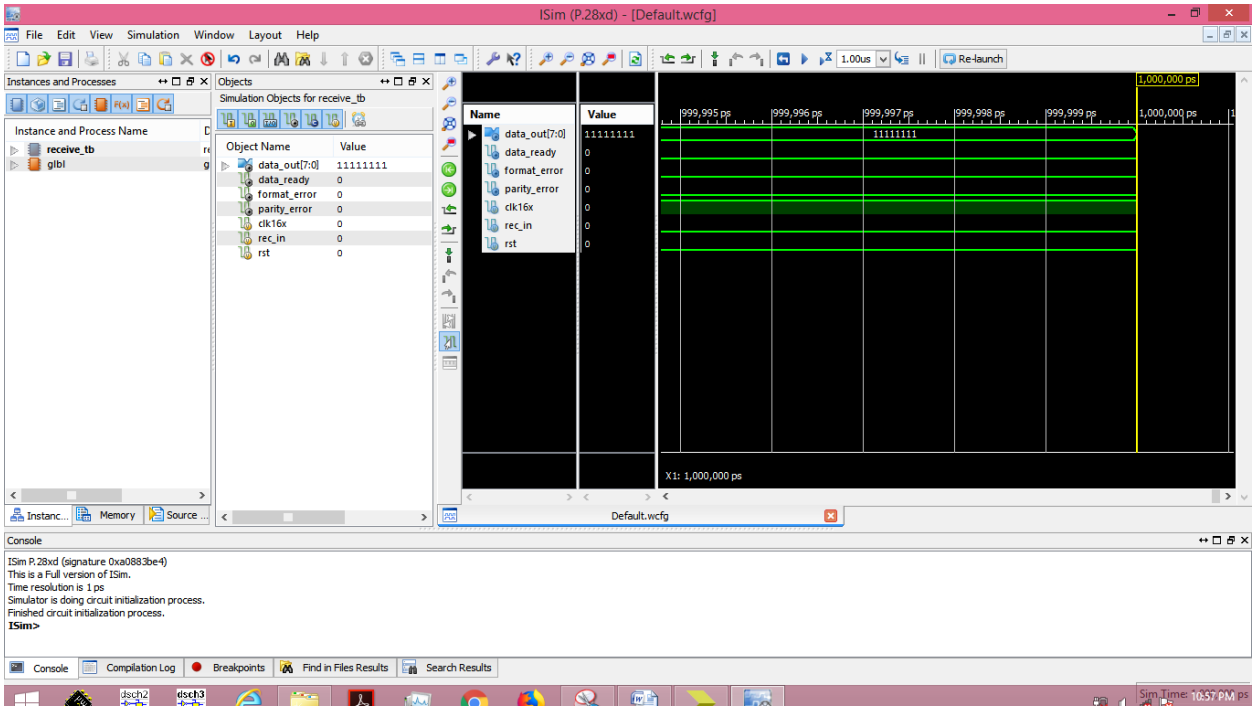
Step 8: SELECT ISIM SIMULATOR and SIMULATE BEHAVIORAL MODEL

If no errors isim window will open



Step 9: ISIM WINDOW

 select zoom to full view



CHAPTER 7

SIMULATION RESULTS

7.1 EXISTING RESULTS

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	1729	17600	9%
Number of fully used LUT-FF pairs	0	1729	0%
Number of bonded IOBs	128	100	128%

FIG 7.1 DESIGN SUMMARY

```
    MUXCY:CI->O           1   0.013   0.000  CPA2/Madd_fsum_cy<56> (CPA2/Madd_fsum_cy<56>)
    MUXCY:CI->O           1   0.013   0.000  CPA2/Madd_fsum_cy<57> (CPA2/Madd_fsum_cy<57>)
    MUXCY:CI->O           1   0.013   0.000  CPA2/Madd_fsum_cy<58> (CPA2/Madd_fsum_cy<58>)
    MUXCY:CI->O           1   0.013   0.000  CPA2/Madd_fsum_cy<59> (CPA2/Madd_fsum_cy<59>)
    MUXCY:CI->O           1   0.013   0.000  CPA2/Madd_fsum_cy<60> (CPA2/Madd_fsum_cy<60>)
    XORCY:CI->O           3   0.251   0.438  CPA2/Madd_fsum_xor<61> (n0538<61>)
    LUT3:I0->O            2   0.043   0.347  CPA5/aa[61].b1/CCC1/Mmux_cout111 (CPA5/C<62>)
    LUT5:I3->O            1   0.043   0.550  CPA5/aa[62].b1/CCC2/Mmux_sum11 (CPA5/sum<62>)
    LUT6:I0->O            1   0.043   0.000  CPA5/Madd_fsum_lut<62> (CPA5/Madd_fsum_lut<62>)
    MUXCY:S->O            0   0.230   0.000  CPA5/Madd_fsum_cy<62> (CPA5/Madd_fsum_cy<62>)
    XORCY:CI->O           1   0.251   0.279  CPA5/Madd_fsum_xor<63> (p_63_OBUF)
    OBUF:I->O                 0.000          p_63_OBUF (p<63>)
    ----------------------------------------
    Total                     6.410ns (2.362ns logic, 4.048ns route)
                                      (36.8% logic, 63.2% route)

==========================================================================
```

FIG 7.2 TIME SUMMARY

Device	
Family	Virtex4
Part	xc4vfx12
Package	ff668
Temp Grade	Commercial
Process	Typical
Speed Grade	-10

Environment	
Ambient Temp (C)	50.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250

Characterization	
PRODUCTION	v1.0,02-02-08

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.004	1	---	---
Logic	0.000	9	10944	0
Signals	0.000	34	---	---
DCMs	0.000	0	4	0
IOs	0.000	21	320	7
Leakage	0.165			
Total	0.169			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	9.3	83.4	51.6

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.074	0.003	0.071
Vccaux	2.500	0.031	0.000	0.031
Vcco25	2.500	0.001	0.000	0.001

	Total	Dynamic	Quiescent
Supply Power (W)	0.169	0.004	0.165

FIG 7.3 POWER SUMMARY

7.2 Proposed Power consumption

Xilinx ISE software was used to create all of the DST-R4BM designs. This software programmed gives two types of outputs: simulation and synthesis. The simulation results provide a thorough examination of the DST-R4BM architecture in terms of input and output byte level combinations. Decoding procedure approximated simply by applying numerous combinations of inputs and monitoring various outputs through simulated study of encoding correctness. The use of area in relation to the transistor count will be accomplished as a result of the synthesis findings. In addition, a time summary will be obtained with regard to various path delays, and a power summary will be prepared utilizing the static and dynamic power consumption.

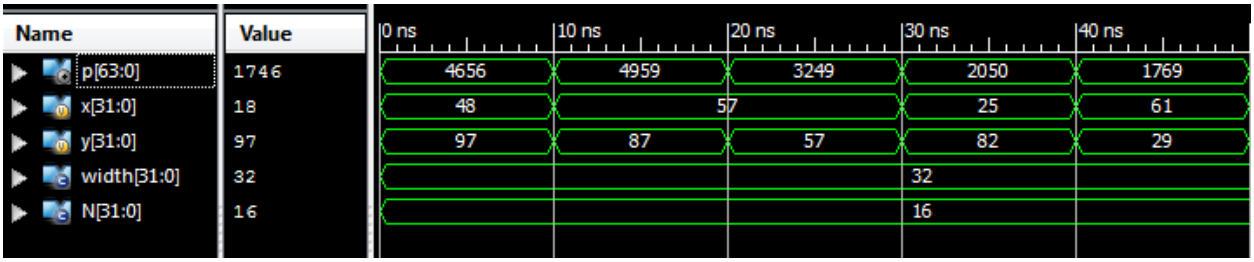


FIGURE 7.4. SIMULATION OUTCOME.

Figure 7.4 shows the simulation results of proposed DST-R4BM. Here, width is the input pin, which is used to change the size of DST-R4BM. So, variable width concept is justified. Further, X and Y are the input data ports and P is the output port.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	1729	17600	9%
Number of fully used LUT-FF pairs	0	1729	0%
Number of bonded IOBs	128	100	128%

FIGURE 7.5. DESIGN SUMMARY.

Figure 7.5 shows the design (area) summary of proposed method. Here, the proposed method utilizes the low area in terms of slice LUTs i.e., 1729 out of available 17600.

```
MUXCY:CI->O           1    0.013   0.000  CPA2/Madd_fsum_cy<56> (CPA2/Madd_fsum_cy<56>)
MUXCY:CI->O           1    0.013   0.000  CPA2/Madd_fsum_cy<57> (CPA2/Madd_fsum_cy<57>)
MUXCY:CI->O           1    0.013   0.000  CPA2/Madd_fsum_cy<58> (CPA2/Madd_fsum_cy<58>)
MUXCY:CI->O           1    0.013   0.000  CPA2/Madd_fsum_cy<59> (CPA2/Madd_fsum_cy<59>)
MUXCY:CI->O           1    0.013   0.000  CPA2/Madd_fsum_cy<60> (CPA2/Madd_fsum_cy<60>)
XORCY:CI->O           3    0.251   0.438  CPA2/Madd_fsum_xor<61> (n0538<61>)
LUT3:I0->O            2    0.043   0.347  CPA5/aa[61].b1/CCC1/Mmux_cout111 (CPA5/C<62>)
LUT5:I3->O            1    0.043   0.550  CPA5/aa[62].b1/CCC2/Mmux_sum11 (CPA5/sum<62>)
LUT6:I0->O            1    0.043   0.000  CPA5/Madd_fsum_lut<62> (CPA5/Madd_fsum_lut<62>)
MUXCY:S->O            0    0.230   0.000  CPA5/Madd_fsum_cy<62> (CPA5/Madd_fsum_cy<62>)
XORCY:CI->O           1    0.251   0.279  CPA5/Madd_fsum_xor<63> (p_63_OBUF)
OBUF:I->O                 0.000          p_63_OBUF (p<63>)
----------------------------------------
Total                     6.410ns (2.362ns logic, 4.048ns route)
                                  (36.8% logic, 63.2% route)

==========================================================================
```

FIGURE 7.6. TIME SUMMARY

Figure 5.6 shows the time summary of proposed method. Here, the proposed method consumed total 6.410ns of time delay, where 2.362ns of delay is logical and 4.048ns of delay is route.

A	B	C	D	E	F	G	H	I
Device			On-Chip	Power (W)	Used	Available	Utilization (%)	
Family	Virtex4		Logic	0.000	63	10944	1	
Part	xc4vfx12		Signals	0.000	132	---	---	
Package	ff668		DCMs	0.000	0	4	0	
Temp Grade	Commercial		IOs	0.000	97	320	30	
Process	Typical		Leakage	0.165				
Speed Grade	-10		Total	0.165				
Environment			Thermal Properties		Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)	
Ambient Temp (C)	50.0				9.3	83.5	51.5	
Use custom TJA?	No							
Custom TJA (C/W)	NA							
Airflow (LFM)	250							
Characterization								
PRODUCTION	v1.0,02-02-08							

FIGURE 7.7. POWER SUMMARY.

Figure 7.7 shows the power consumption report of propsoed DST-R4BM. Here, the DST-R4BM consumed power as 0.165 watts. Table 7.1 compares the performance evaluation of various DST-R4BM controllers. Here, the propsoed DST-R4BM resulted in superior (reduced) performance in terms of LUTs, time-delay, and power consumption as compared to conventional approaches such as TABM [20] , HSAM [22], and R16BM [24].

TABLE 7.1. PERFORMANCE EVALUATION.

Metric	TABM [20]	HSAM [22]	R16BM [24]	Proposed HML-BIST
LUTs	7523	5642	4834	1729
Time delay (ns)	11.28	8.284	7.453	6.410
Power consumption (w)	3.49	2.34	1.349	0.165

CHAPTER 8

CONCLUSION

The design and implementation of a variable width Radix-4 booth multiplier using DST are the main goals of this work. The radix-4 modified booth encoding method was used to create the partial products. Additionally, the reduced stages of a recoding adder are used to add the partial products bits in parallel. The simulation showed that the proposed DST-R4BM performed better than conventional multipliers in terms of area, delay, and power. Further, this work can be extended with multiply and accumulation unit for deep learning neural network modulators.

8.1 FUTURE SCOPE

The process of multiplication predominates in many applications of digital signal processing (DSP) and machine learning; for instance, more than 90 percent of the computations performed by convolutional neural networks (CNN) are filled by multiply-accumulate (MAC) operations. Because of this, the multiplier is a crucial component in a wide variety of different hardware systems. The traditional method of multiplication consists of three main stages. (1) The partial products are generated by multiplying two inputs, which are referred to as the multiplier and the multiplicand (PPs). (2) Creating two rows out of the PPs matrix with the use of partial product reduction strategies (3) The addition of the last two rows of PPs was propagated by the last carry, which occurred before the addition. Specifically, the second phase is responsible for a large amount of the total performance, as well as cost and power usage. Therefore, the radix-4 Booth method has the potential to increase the performance of multiplication due to the fact that the radix-4 Booth multiplier has the ability to cut the number of PP rows in half.

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