A

Major Project Report

On

IMPLEMENTATION OF HYBRID MEDIAN FILTERING USING HYBRID DATA COMPARATORS

Submitted

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In Partial Fulfillment of the requirements for the Award of Degree of

MASTER OF TECHNOLOGY

IN

VLSI SYETEM DESIGN

Submitted

By

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Kandlakoya, Medchal Road, R.R. Dist. Hyderabad-501401

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CERTIFICATE

This is to certify that the project entitled "**IMPLEMENTATION OF HYBRID MEDIAN FILTERING USING HYBRID DATA COMPARATORS**" is a bonofide work carried out by Mylaram Nikhitha (208R1D5710) in partial fulfillment of the requirement for the award of the degree of MASTER OF TECHNOLOGY in ELECTRONICS AND COMMUNICATION ENGINEERING from CMR Engineering College, affiliated to JNTU, Hyderabad, under our guidance and supervision.

The results presented in this project have been verified and are found to be satisfactory. The results embodied in this project have not been submitted to any other university for the award of any other degree or diploma.

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DECLARATION

This is to certify that the work reported in the present project entitled "**IMPLEMENTATION OF HYBRID MEDIAN FILTERING USING HYBRID DATA COMPARATORS**" is a record of Bonofide work done by me in the Department of Electronics and Communication Engineering College, JNTU Hyderabad. The reports are based on the project work done entirely by me and not copied from any other source. I submitted my project for further development by any interested students who share similar interests to improve the project in the future.

The results embodied in this project report have not been submitted to any other University or Institute for the award of any degree or diploma to the best of our knowledge and belief.

Mylaram Nikhitha

(208R1D5710)

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Apart from the efforts of me, the success of this project depends largely on the encouragement and guidelines of many others. I take this opportunity to express my gratitude to the people who have been instrumental in the successful completion of this project.

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CONTENTS

ABSTRACT

Filters are used to remove the different types of noises including salt and pepper, gaussian, and random noises from image. Therefore, the VLSI oriented hardware implementation of filters plays the crucial role in real time applications. However, the conventional hardware-based filters are failed to reduce the look-up-table (LUT)s, path delays, and power consumption. Therefore, this work is focused on implementation of Hybrid Median Filter (HMF) using Data Comparator (DC) logic. Initially, the multiplexer selection logic-based data comparator is used to identify the high and low values from two numbers. Then, data comparator is repeated for multiple number of times for nine pixels combinations, which identifies the median value from nine pixels. The subjective and objective evaluation shows that the proposed HMF-DC resulted in superior performance in terms reduced noise, hardware metrics like LUTs, delay, and power consumption as compared to state of art approaches.

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBRIVATIONS

SRAM	-	Serial Random Access Memory
ECC	-	Error Correction Codes
SEC-DEC	-	Single Error Correction – Double Error Detection
MCU	-	Multiple Cell Upset
OLS	-	Orthogonal Latin Square
DS	-	Different set
AROF	-	Adaptive Rank Order Filter
DROF	-	Decision Rank Order Filter
DTBDM	-	Decision Tree Based De-noising Method
CBL	-	Common Boolean Logic
SMF	-	Standard Median Filter
DMF	-	Dynamic Median Filter
AMF	-	Adaptive Median Filter
BLAC	-	Barrow Look Ahead Logic
CBC	-	Conventional Bitwise data Comparator
CSLC	-	Carry Select Logic data Comparator
DDC	-	Decoder based Data Comparator
MDC	-	Multiplexer based data Comparator
2BEC	-	Twos complement comparator using Binary to excess one converter
BEC	-	Binary to Excess one Converter
MSS	-	Modified Shear Sorting
HMF-DC	-	Hybrid Median Filter-Data Comparator
HVL	-	Hardware Verification Language
OVI	-	Open Verilog International
CDV	-	Coverage Driven Verification
LUT	-	Look Up Table

CHAPTER-1

INTRODUCTION

1.1 INTRODUCTION

Comparator networks are abstract devices used in the field of computer science. They are composed of a set number of wires that carry values and comparator modules that connect pairs of wires and swap the values on the wires if they are not in the desired order. Comparator networks are used to compare two sets of data. Sorting networks are the term given to such networks when they are intended to sort a certain number of values. In most cases, the number of values to be sorted is set. Sorting networks are distinct from generic comparison sorts in two key respects: first, they are unable to process inputs of an arbitrary size; second, the order in which comparisons are performed in sorting networks is predetermined and is not influenced by the results of earlier comparisons. Because comparison sequences are independent of one another, parallel processing, and the implementation of comparisons in hardware are both made easier.

Sorting nets are deceptively simple, but the science behind them is surprisingly deep and intricate. Around the year 1954, Armstrong, Nelson, and O'Connor began their research on sorting networks, which led to the eventual patenting of the concept. The implementation of sorting networks may take place in either the hardware or the software. Donald Knuth explains how the comparators for binary integers may be built as simple electrical devices that have three states each. Batcher proposed utilizing them in 1968 as a potential replacement for both buses and the quicker and more costly crossbar switches when it came to the construction of switching networks for computer hardware.

Sorting nets, and particularly bitonic merge sort, have been use by the GPGPU community since the early 2000s with the purpose of developing sorting algorithms that can be executed on graphics processing units. In applications as diverse as data mining and database management, automated teller machines and communication switching, scientific computing and scheduling, artificial intelligence and robotics, image, video, and signal processing, and more, sorting is an essential step in the process. Sorting is often carried out in hardware with the use of application-specific integrated circuits or field-programmable

gate arrays when it is necessary for the application to have a high level of performance. The configuration of the hardware sorting units might look quite different depending on the applications that are intended for use with them. Some applications of image processing, such as median filtering, may have as few as nine inputs, while others can have as many as tens of thousands. The number of inputs can go as low as nine or as high as tens of thousands. Sometimes the data inputs are integers, floating-point numbers, or binary values, and their precision may range anywhere from four bits to 256 bits.

The most important considerations about hardware implementations are the costs of the hardware and the amount of power it uses. In many different contexts, the overall area of the chip is restricted. Because of the exponential relationship between temperature and leakage current, one of the most significant goals in the scaling of fabrication methods is to maintain chip temperatures as low as possible. The amount of power that is used must be reduced to the minimum practicable. An essential objective involves the research and development of hardware-based sorting methods that are both cost and power efficient.

The most common method is to set up what is known as a Batcher (or bitonic) network, which involves interconnecting a series of compare and swap (CAS) units. Pipelining is a simple process that may be performed on such networks. The fact that hardware-based solutions are parallel in nature gives them a performance advantage over sequential software-based solutions. Both the cost of the hardware and the amount of power used are determined by the total number of CAS blocks as well as the cost of each individual CAS block.

1.2. OBJECTIVE

The primary purpose of the work that is going to be done is to create a new data comparator that provides an affordable answer to the problem of ranking or sorting networks according to their speed, power, and total area. Circuits are sorted with its assistance. We are currently designing a CAS Median Filter that can accommodate a wide range of filter sizes. Recently, we have begun the process of designing a median filter utilizing our proposed design. The typical method involves wiring up a network of compare and-swap (CAS) having hardware cost and the power consumption depend on the number of CAS blocks and the cost of each CAS block.

1.3 CHALLENGES

The typical method involves wiring up a network of compare and-swap (CAS). This article presents a unique technique to sorting networks based on "shear sorting utilizing Three Cell Sorter," which is designed to be both area-efficient and power-efficient.

1.4 EXISTING SYSTEM

In Existing System, a stochastic processing algorithm was introduced. This algorithm was based on uniformly distributed random bit streams. In this computer paradigm, each digit has the same amount of significance. The range of possible numbers is constrained to be between 0 and 1, and each number is encoded according to the likelihood of receiving a one rather than a zero from the stream. Conventional Design is what's called for when it comes to the CAS Network's planning and design.'

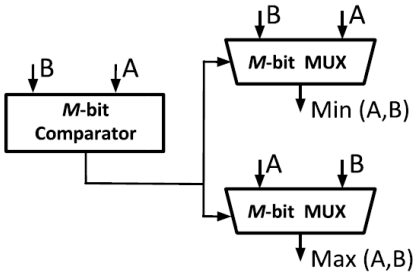


Fig 1.1: - Existing method

EXISTING SYSTEM TECHNIQUE:

- Conventional binary design

EXISTING SYSTEM DRABACKS:

- Less compact
- High Cost
- Less Accuracy

CHAPTER-2

LITERATURE SURVEY

2.1 LITERATURE SURVEY ON MEDIAN FILTERS

The comparator is a combinational circuit that is used in the process of determining if the binary number that is present at one input is larger or less than the binary number that is present at another input. Comparators are critical components, and an XOR gate may serve this purpose. The Comparators may be broken down into two distinct categories (a). Magnitude Comparator (b). Data Comparator. In the first method, just the magnitude of the two binary integers is compared, but in the second method, both the larger and the lesser data are provided.

The Magnitude comparator has two outputs, one of which indicates if the first input is larger than the second input, while the other output indicates the opposite. In contrast, a data comparator is also often called a two-cell comparator since it compares two words, X and Y, and returns a number that is either higher or lower depending on which word is being compared. A compact, high-quality, cost-effective, high-performance, and low-power comparator plays a vital role in almost all hardware comparators. The purpose of this study is to investigate the characteristics of certain comparator circuits that, in comparison to those of existing circuits, provide superior performance.

An Adaptive Rank Order filter (AROF) with VLSI implementation has been created by in [1] to eliminate impulse noise and pipelining with parallel processing in order to speed up the filtering process. This filter was designed to reduce impulse noise. In comparison to the Decision Tree Based De-noising Method, the benefit of the Decision Rank Order Filter (DROF) is that it takes up less space and also has a design that is easy to understand (DTBDM). One of the drawbacks of VLSI DTBDM is that it requires an excessive number of designs for the detection of noise and the reconstruction of noisy pixel.

In [2] investigated the possibility of designing a comparator that is both high speed and low power. This is possible because the comparator runs using just 1volt of power, has a shorter propagation delay, and its architecture comprises a two-stage CMOS op-amp

circuit. This study involves the development of a comparator using a cadence tool that has a technology of 0.18 micrometers.

In [3] presented a unique category of comparators, and the simulation of these circuits in LTspice-IV made use of PTM 45nm technology. The supply voltage for these circuits was set at 1 volt DC. It runs at a greater speed and provides a more stable output in comparison to 90nm and 180nm comparators, unlike the static and dynamic features of all of these comparators, which are studied and compared below.

In [4] produced a variety of different designs in order to lessen the amount of space and power that was used. This was done since even a little reduction in the amount of space and power that a circuit uses may result in a significant overall cost reduction. When compared to an automatically produced design, full-custom design results in around a 50% reduction in area and a 35% reduction in power usage, according to the study.

In their work on improved shear sorting, In [5] established a parallel design in addition to a pipelined architecture. This approach included a space-saving data comparator for the classification of 9 different components. The area optimized two cell sorter is the fundamental component of the processing system. A three cell sorter is formed by the combination of a group of three two cell sorters, and this sorter employs a compare and swap strategy in order to arrange the data sequence.

In [6] created a set of VLSI algorithms and implementation designs for a family of nonlinear filters. Keeping chan was involved in this research. All of the functions that were previously specified by stack filters are included in the class of filters; the rank-order filter and the median filter are special examples of this class. Utilizing a single binary processing circuit in a recursive manner k times may allow the function of a stack filter to be accomplished. A unique Borrow Look Ahead Logic based Comparator (BLAC) was presented in [7] and its output was implemented. An architecture of modified shear sorting that is pipelined as well as parallel.

In [8] authors presented a VLSI design for decision-based asymmetrical trimmed midpoint filter that was based on a finite state machine. A innovative approach for locating the median value of a set was suggested, and it included employing modified selection sort. A brand new 8-bit data comparator that made use of carry select logic was presented in [9].

The bit-serial architecture that has been presented is one that lends itself extremely well to VLSI implementation.

We describe a unit that is capable of doing continuous-time hybrid approximation computing. In this model, both analog and digital signals are treated as functions of continuous time. In every analog and mixed-signal block, you'll see the utilization of digitally aided calibration. Because of technological scalability and significant usage of class-AB analog blocks, our device is capable of arbitrary nonlinearities and achieves power dissipation that is 16 times lower than that of the previous art. Depending on the specifics of the equation, the device can typically achieve a computational accuracy of about 0.5% to 5% RMS, solution times ranging from a fraction of one microsecond to several hundred microseconds, and total computational energy ranging from a fraction of one nanojoule to hundreds of nanojoules.

In the SC paradigm [11], logical processing is carried out on bit streams that have been randomly generated. In previous research, streams were formed using linear feedback shift registers. These registers were a substantial contributor to the overall cost of the hardware and used up a considerable amount of power. In this piece of research, a novel method for encoding signal values is presented: the calculation is carried out on analog periodic pulse signals. Adjusting the frequency and duty cycles of pulse width modulated (PWM) signals allows for the generation of time-encoded signals that correspond to certain values. This is accomplished via the use of pulse width modulation.

The capacity to gracefully [12] noise and the skew tolerance are the key benefits that come with using stochastic computing. Another advantage is the extremely basic hardware requirements that are needed to accomplish sophisticated operations. However, this paradigm's very significant latency presents a possible obstacle to its wider use, especially in circumstances that call for a high level of precision. This research presents a novel method that is high-speed while still being accurate for the implementation of stochastic circuits. This method makes use of synchronized analog pulses as a new method for encoding correlated stochastic numbers.

One of the most efficient oblivious parallel sorting [13] algorithms that has been discovered to date is called bitonic sort. The great degree of modularity that bitonic sort

has enables it to be mapped to a variety of different connectivity networks. This article presents a mapping of the bitonic sort algorithm to the chained-cubic tree (CCT) connectivity network. The BSCCT algorithm's performance in terms of calculation time, communication cost, message latency, and key comparisons is evaluated with the assistance of simulation, which is developed and employed in the process. When 1024 processors were utilized to sort 32 million keys, simulation results indicated that the BSCCT algorithm achieved a speedup that was nearly 12-fold greater than a bitonic sort on a single CPU. This was the case when comparing the two methods for sorting data.

Sorting that is both high-throughput and low-latency [14] is a crucial need in many applications because of the vast volumes of data that they deal with. This study demonstrates effective strategies for the construction of sorting units that have a high throughput and a low latency. The modular design principles that we use for our sorting architectures allow us to develop larger sorting units by constructing them hierarchically from smaller building pieces.

Since this is a situation that frequently arises in many applications for scientific computing, data mining, network processing, digital signal processing, and high-energy physics, the sorting units have been optimized for situations in which only the M largest numbers from N inputs are required. This is because this situation commonly occurs in these types of applications. In order to create parameterized, pipelined, and modular sorting units, we make use of the methodologies that we have described.

In this synopsis, we provide two novel concurrent error-detection (CED) [15] techniques for a class of sorting networks, such as odd-even transposition, bitonic, and perfect shuffle sorting networks. These strategies are designed to identify errors in the networks simultaneously. In order to do an analysis of the fault coverage, a probabilistic approach has been created, and the overhead of the hardware has been assessed.

The first thing that we do is suggest a CED system that can identify any and all mistakes that are brought on by individual faults in a concurrent checking sorting network. This strategy is the first one that has been developed that uses a significant amount less hardware overhead than duplication while maintaining the same level of performance.

A cutting-edge hierarchical sorting network that can tolerate defects is given [16]. The area-time cost of the bitonic sort and the odd-even transposition sort are both taken into account in the design, which results in a balanced solution. It decreases the wiring complexity of the bitonic sorter in VLSI or WSI (wafer scale integration) implementation, and it consumes less hardware than a single-level odd-even transposition sorter.

In order to reduce the hardware overhead as much as possible, we first determine the best number of levels in the hierarchy, and then we determine the sorting capacity of each level. Because of the very regular nature of the hierarchical sorting network, it is not difficult to implement redundancy at each and every level of the hierarchy.

In the process of implementing hierarchical reconfiguration, the faulty cells at the lowest level are initially replaced with spare cells. If there is not enough redundancy at the level that is currently being worked on, the process moves up to the next higher level to execute reconfiguration.

2.2 Literature Survey On Data Comparators

In spatial domain filtering, the image pixel values are directly manipulated to achieve the desired result. Available spatial domain filters are mean, order statistics and adaptive filters [17]. Image filters have wide applications in the domain of image processing, satellite, and remote sensing, medical and microscopic imaging, geographic image surveillance and seismographic analysis.

In [18] authors proposed a new method of median filter by sharing Common Boolean Logic (CBL) which replaces RCA-XOR gate and inverter are used for the sum generation. AND gate and OR gate is used for carry generation [19]. Based on the specific carry input given to the multiplexer both the required sum and carry output are generated. An efficient design is proposed by partial sharing of the circuit and by logical simplification. This design leads to a decrease in the transistor count with minimum power dissipation.

In [20] authors proposed the efficient Frequency Domain Denoising Filters by using a newly proposed new type of basic full adder. In [21] authors discussed about the implementation of median filter using basic logic gates. The main advantage of using the

basic gates is its zero-power dissipation under ideal conditions. Design modifications are performed in the basic gates to reduce the garbage bits and constant inputs.

In [22] authors proposed a proficient Efficient Median Filter which replaces a BEC with normal Boolean logic in conventional CSLA. This work utilizes an effective CSLA by sharing the Common Boolean logic term [23]. One OR gate and one inverter are used for carry and sum generation. Multiplexer is used for selecting the required output based on appropriate carry. Power and delay are reduced with increase in area.

In [24] authors proposed a low-cost image denoising standard median filter (SMF**)** methodology using CSLA without multiplexers. First carry input zero operation is performed followed by BEC adder operation. The circuit is designed such that BEC adder replaces the last MUX arrange utilized in customary methodology. Replacing the MUX stage will lessen the area and delay to give considerably higher execution for the adder.

In [25] authors implemented parallel pipeline median finder using ultra low power design in near threshold region. Sub threshold operation is similar to minimum energy operation. This work deals with the energy delay modeling framework that develops in the weak, moderate and strong inversion regions. The operation below the minimum energy point is also discussed [26]. The experimental results show that there is a 20% increase in energy which leads to better performance. This concept is used for comparing adders based on their energy delay characteristics and presents the results for our estimation technique.

In [27] authors discuss area, power and delay performances of hybrid sorting-based dynamic median filtering (DMF) by using different CMOS logic styles. A new hybrid style is proposed for designing full adder. Though full adders are used in tree structured arithmetic circuits [28], new hybrid logic is used for simulation which is used in the application environment. A full swing and balanced output are achieved using this logic. An area efficient layout is achieved by this methodology.

In [29] authors designed low power median filter based on the variation in supply voltage for impulse noise suppression. Based on input vector pattern, supp.ly voltage is selected. This method will drastically reduce the power consumption [30]. This methodology is explained with respect to the prototype of 32-bit RCA. Simulation results

show that there is a 29% reduction in power requirement when compared with conventional RCA.

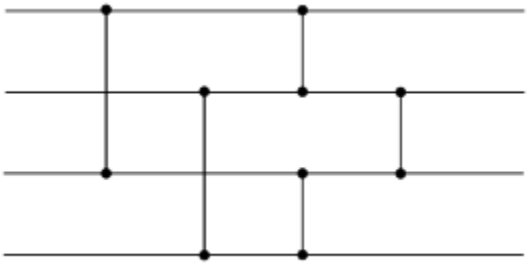
In [31] authors designed adaptive median filter (**AMF)** with thresholding methods for low power applications. Designing the structure with single supp.ly voltage or comparison based on the gate count is not a suitable method for finding the optimal structures. Therefore, high performance structures should be combined with the supp.ly voltage scaling for obtaining a reduced energy. These technology outlooks the traditional design for low power operation.

CHAPTER 3

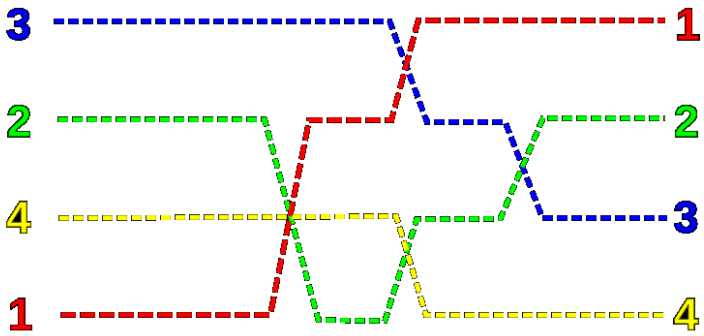
BASICS OF DATA SORTING

3.1 GENERAL

Comparators and wires are the two components that make up a sorting network. Comparators are used to compare two different objects. It is common practice to see the wires as moving in a left-to-right direction, carrying values (one on each cable) that move across the network in unison. Every comparator has two wires that it connects. When a comparator comes into contact with a pair of values that are going via a pair of wires, the comparator will switch the values if and only if the value of the top wire is higher than the value of the bottom wire. In a formula, if the top wire carries x and the bottom wire carries y, then after hitting a comparator the wires carry {\display style x'=\min(x, y)} x' = \min(x, y) and {\display style y'=\max(x,y)} y' = \max(x, y), respectively, so the pair of values is sorted. [5]:635 The term "sorting network" refers to a network that is comprised of wires and comparators that can accurately sort all conceivable inputs into ascending order. The following diagram illustrates the whole functioning of a simple sorting network. It is not difficult to see why this sorting network would appropriately sort the inputs; observe that the first four comparators will "sink" the biggest value to the bottom and "float" the smallest value to the top of the list. The last comparator does nothing more than separate the two wires in the center.



(a)



(b)

Fig 3.1: - One way sorting

3.2 COMPARATOR

A digital comparator, also known as a magnitude comparator, is a piece of electrical gear that compares the magnitudes of two numbers by comparing them in binary format. The device can decide if one number is larger than, less than, or equal to the other number. The Three Cell Sorter is a Combination of Three and Two Data Comparators.

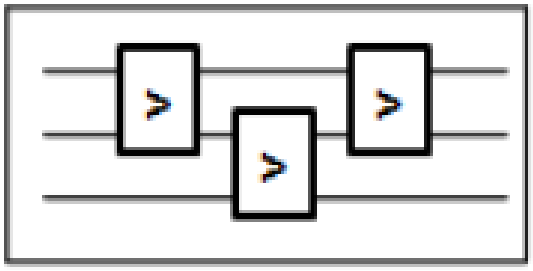


Fig 3.2: - Data comparator

CAS BLOCK – SHEAR SORTING: The procedure of modified shear sorting is put into action by using a compare and swap operation that functions as a parallel architecture. To construct a more compact processing element known as a three-cell sorter, a distinct design for the data comparator, which is also known as a two-cell sorter, is required. A three-cell sorter is a fundamental unit that evaluates three components and provides information on the maximum, median, and lowest value of those three

components. These three cell sorters make up the fundamental processing component of the Modified Shear sorting procedure.

The basic action of a parallel architecture is known as a two-cell sorter, and the processing element of these architectures is known as a three-cell sorter. This is due to the fact that a three-cell sorter is equivalent to three separate two-cell sorters. In this design, in order to establish the median value of the nine components that are provided by the use of the sorting approach, it is fundamentally necessary to have a network. The Architecture shown in fig below is used with seven different three-cell sorters in order to carry out the operation either in rows, columns, or right diagonals, each of which has nine individual components. It is clear, as seen in the image, that we employ three different sets of three-cell sorters in order to arrange the three components of the row and column in ascending order.

Cas Block – In the Conventional Format

Therefore, the price of the sorting network's hardware is directly proportional to the total number of CAS blocks as well as the price of each individual block. Each CAS block is made up of one M-bit comparator and two M-bit multiplexers, as can be seen in the figure below, which depicts a weighted binary architecture with a data width of M bits. Therefore, elevating the resolution of the data will result in a rise in the level of intricacy shown by the design. The increased complexity of the design has a direct impact on the total cost of the hardware implementation, as well as on latency, power, and ultimately, energy consumption.

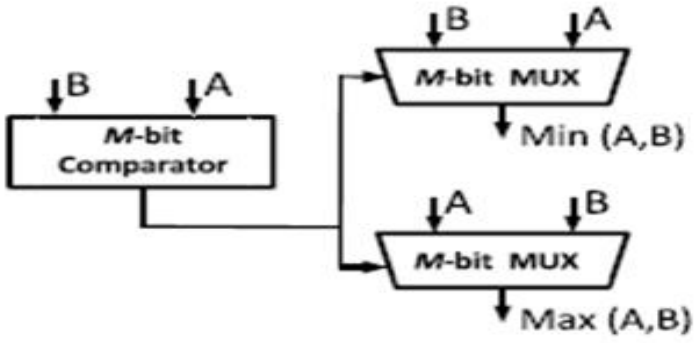


Fig 3.3: - Block diagram of conventional data comparator

Cas Network For A 3×3:

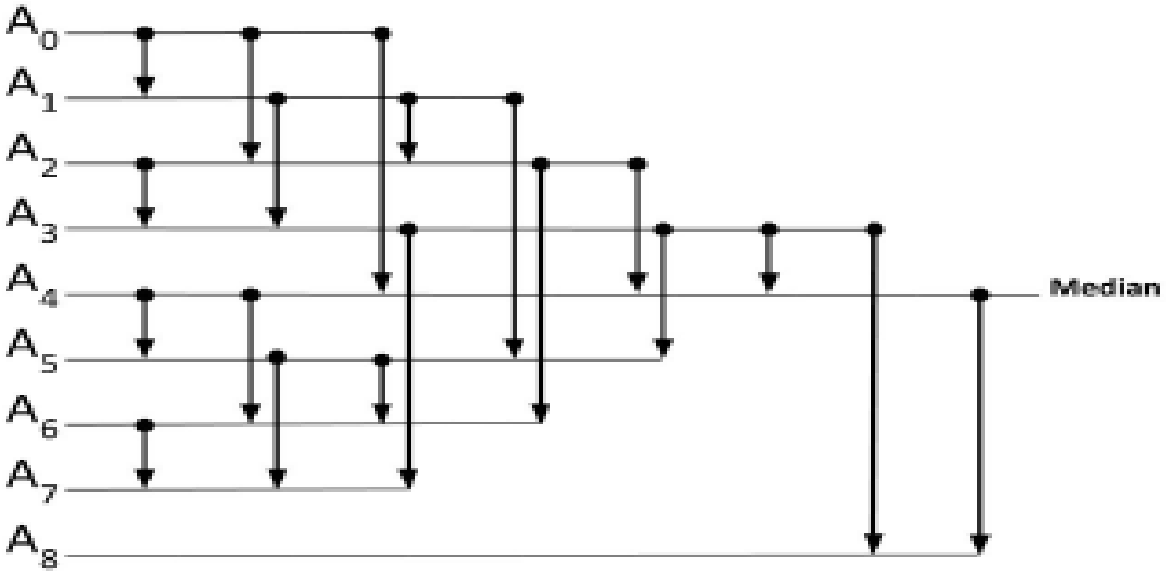


Fig 3.4: - CAS network design for 3x3 input and one median output

Multiplexers:

A multiplexer, often known as a mux, is a piece of electronic equipment that can accept either analog or digital signals as input and then combine the chosen signal into a single transmission line. A multiplexer with 2n inputs will have n select lines, and these lines will be used to choose which of the input lines will be sent to the output.

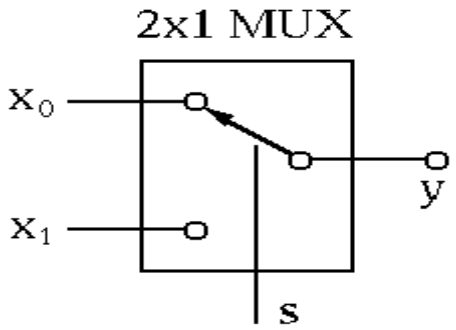


Fig 3.5: - 2 x 1 Multiplexer

M-Bit Input Register: M-Bit Register Consist of M-Flip Flops. A flip-flop is an example of a one-bit memory cell that may use for the purpose of storing digital data. We will need to use a group of flip-flops to boost the storage capacity in terms of the total amount of

bits. A Register is a collective noun for this kind of flip-flop assembly. The n-bit register will be made up of an n-number of flip-flops, and it will have the capacity to store an n-bit word.

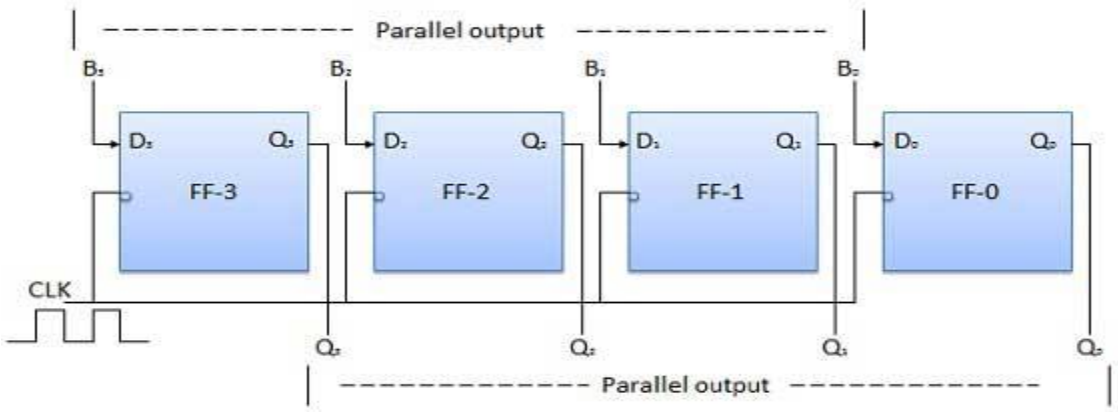


Fig 3.6: - M-bit register

3.3 SORTING NETWORKS

In the search for efficient techniques of sorting, a variety of networks have been developed that can sort n items in a period that is much shorter than Q. (n log n). A comparison network model serves as the foundation for these sorting networks. In this approach, numerous comparison operations are carried out concurrently. The comparator is the fundamental building block of these networks. A device known as a comparator is one that has two inputs in the form of x and y, as well as two outputs in the form of x' and y'. For a comparator that increases, x' should equal the minimum value of x and y, while y' should equal the maximum value of x and y. On the other hand, a comparator that decreases should have x' equal the maximum value of x and y. The graphical depiction of the two different kinds of comparators may be seen in Figure 9.3. Before the two components may proceed to the comparator's output wires, they are first compared as soon as they are received by the comparator's input wires, and then, if required, they are switched. A comparator that is decreasing is denoted by, while a comparator that is growing is denoted by. In most cases, a sorting network will consist of several columns, and each column will have several comparators that are linked in parallel to one another. Each column of comparators executes a permutation, and the output that is generated from the last column

is then sorted in either ascending or descending order, depending on the user's preferences. The usual distribution of the sorting network is seen in figure 9.4. The number of individual rows that make up a network is referred to as its depth. Because the speed of a comparator varies depending on the technology being used, the depth of a network has a direct bearing on the pace at which it operates.

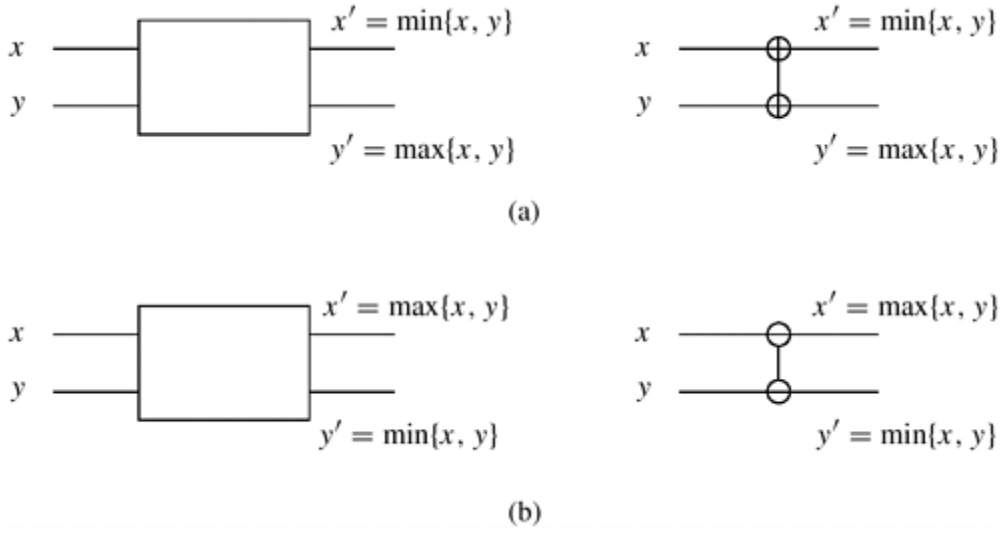


Fig 3.7: - A depiction in schematic form of two types of comparators: a rising comparator (a) and a decreasing comparator (b).

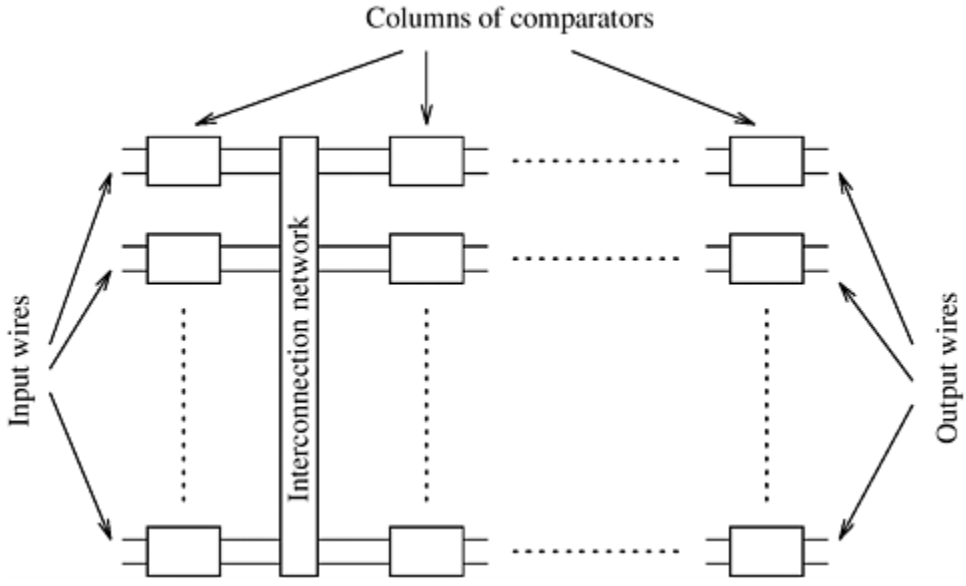


Fig 3.8: - A common network used for sorting.

Every sorting network consists of a series of columns, and inside of each column is a number of comparators that are linked together in parallel.

By simulating the comparators in software and carrying out the comparisons of each column in a sequential fashion, it is possible for us to transform any sorting network into a sequential sorting algorithm. A compare-and-exchange procedure, in which x and y are compared to one another and then switched places if required, is used to simulate a comparator.

The next section provides an explanation of a sorting network that can sort n items in a time that is proportional to log2 n. To keep the presentation as straightforward as possible, we will assume that n is a power of two.

The Bitonic Order

A bitonic sorting network can sort Q(log2 n) items in the same amount of time as sorting n elements. The conversion of a bitonic sequence into a sorted sequence is the most important step in the process carried out by the bitonic sorting network. A bitonic sequence is a sequence of elements with the property that either (1) there exists an index I_0 I_1, such that a_0,..., a_i > is monotonically increasing and a_{i+1},..., a_{n-1}> is monotonically decreasing, or (2) there exists a cyclic shift of indices such that (1) is satisfied. A bitonic sequence can also have the property that (1) and (2) are both satisfied. For instance, the number sequence "1, 2, 4, 7, 6, 0" is a bitonic sequence since it starts off by increasing and then gradually becomes less. In a similar vein, the sequence 8, 9, 2, 1, 0, 4> is also a bitonic sequence since it represents a cyclic shift of the sequence 0, 4, 8, 9, 2, 1>.

A technique for rearranging a bitonic sequence to get a sequence with monotonically rising elements is shown here. Consider the bitonic sequence denoted by s = a_0, a_1, …. a_{n-1}>. This sequence must satisfy the conditions that a_0 a_1... $a_{n/2-1}$ and $a_{n/2}$ $a_{n/2+1}$... a_{n-1}. Take into consideration the subsequences of s shown below:

Equation

There is an element in the series s_1 called b_i = min 'a_i, $a_{n/2+i}$' that is defined in such a way that all the elements that come before b_i are drawn from the growing portion of the original sequence, and all the elements that come after bi are drawn from the shrinking

portion. In addition, the element at sequence s_2 is in such a position that all of the elements that came before it came from the portion of the original sequence that went in a decreasing direction, and all of the elements that came after it came from the portion that went in an increasing direction. The sequences s1 and s2 are both examples of bitonic sequences for this reason. In addition, each individual component of the first sequence has a lesser size compared to each individual component of the second sequence. The reason for this is because b_i is larger than or equal to all the components that make up s1, is equal to or less than all of the elements that make up s2 and is greater than or equal to b_i. As a result, the original challenge of rearrangement a bitonic sequence of size n has been reduced to that of rearrangement of two bitonic sequences of a lesser size, followed by the concatenation of the results. The process of dividing a bitonic sequence of length n into the two bitonic sequences indicated by equation is referred to as a bitonic split. Although we assumed that the initial sequence had rising and decreasing sequences of the same length to achieve s1 and s2, the bitonic split operation is valid for any bitonic sequence. This was done so that we could obtain s1 and s2.

We may iteratively construct shorter bitonic sequences for each of the bitonic subsequences until we acquire subsequences of size one. This process will continue until we have subsequences of size one. After that point, the output is sorted into an ascending order that never stops going higher. Because the size of the issue is cut in half after each bitonic split operation, the number of splits that are necessary to transform the bitonic sequence into a sorted sequence is proportional to log n. The operation known as "bitonic merge" refers to the process of sorting a bitonic sequence by employing bitonic splits. figure 3.8 provides a visual representation of the recursive bitonic merging technique.

Original sequence	3	5	8	9	10	12	14	20	95	90	60	40	35	23	18	0
1st Split	3	5	8	9	10	12	14	0	95	90	60	40	35	23	18	20
2nd Split	3	5	8	0	10	12	14	9	35	23	18	20	95	90	60	40
3rd Split	3	0	8	5	10	9	14	12	18	20	35	23	60	40	95	90
4th Split	0	3	5	8	9	10	12	14	18	20	23	35	40	60	90	95

Fig 3.9: - Combining a bitonic sequence consisting of 16 elements by performing several logs 16 bitonic splits.

A mechanism has been developed that allows us to combine a bitonic sequence with a sorted sequence. The implementation of this technique on a network of comparators is straightforward. depicts this "bitonic merging network," which is a network of comparators also known as "a bitonic merging network." In all, there are log n columns in the network. Each column in the table conducts one stage of the bitonic merging and has n/2 comparators stored inside it. This network accepts the bitonic sequence as its input and outputs the sequence in the correct order after sorting it. BM[n] is the notation that we use to refer to a bitonic merging network that has n inputs. The input will be sorted into monotonically decreasing order if we replace the comparators with comparators. Such a network is indicated by the symbol BM[n].

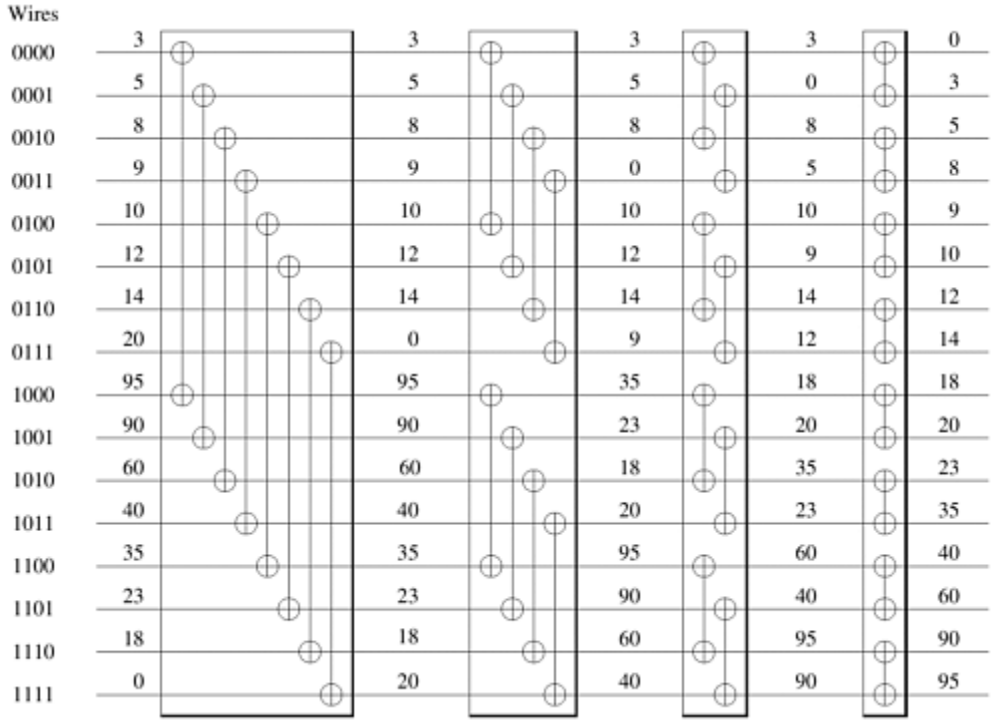


Fig 3.10: - Bitonic merging network

A bitonic network for merging with n equal to 16. The input wires are labeled with the digits 0 through n minus 1, and the binary representations of these values are shown. Each column of comparators is shown on its own independent sheet, and the whole graphic is meant to represent a bitonic merging network for BM. The bitonic sequence is input into the network, and the network returns it in the correct order.

Consider the challenge of sorting n items without any order using the bitonic merging network at your disposal. To do this, many bitonic sequences of progressively longer lengths are merged below figure.

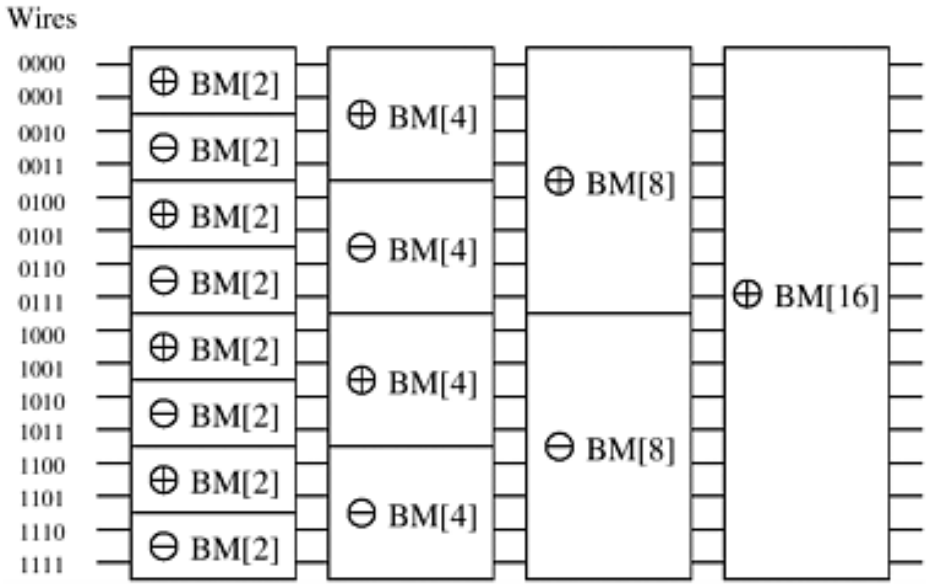


Fig 3.11: - Block diagram of bitonic merging network

A depiction in the form of a schematic of a network that can transform a series of input data into a bitonic sequence. For the sake of this illustration, the notation BM[k] and BM[k] refer to bitonic merging networks of input size k that make use of and comparators, respectively. The input is sorted by the final merging network, which is denoted by BM [16]. n equals 16 in this illustration.

Let us now examine the operation of this procedure. It is possible for a sequence of two elements, x and y, to form a bitonic sequence in one of two ways: either x y, in which case the bitonic sequence has x and y in the increasing part and no elements in the decreasing part, or x y, in which case the bitonic sequence has x and y in the decreasing part and no elements in the increasing part. In either case, the bitonic sequence has x and y in the increasing part and no elements Therefore, every sequence of elements that has not been sorted is a concatenation of bitonic sequences with a size of two. At each level of the network shown in contiguous bitonic sequences are merged in ascending and descending order, respectively. A bitonic sequence is a sequence that may be created by concatenating a growing sequence with a decreasing sequence to create a new sequence. This is the

definition of a bitonic sequence. As a result, the output of each step in the network shown in above figure is a concatenation of bitonic sequences that are longer by a factor of two than those that are present at the input. When we merge bitonic sequences that are bigger and larger, we will finally have a bitonic sequence of size n. Merging the input with this sequence will sort the data. Bitonic sort is the name that we give to the algorithm that is implemented in this approach, and we call the network a bitonic sorting network. In figure 3.9, we see a more detailed representation of the first three phases of the network that we saw in figure 3.7. The culmination of the process shown in figure 3.7 may be seen in full detail in figure 3.6.

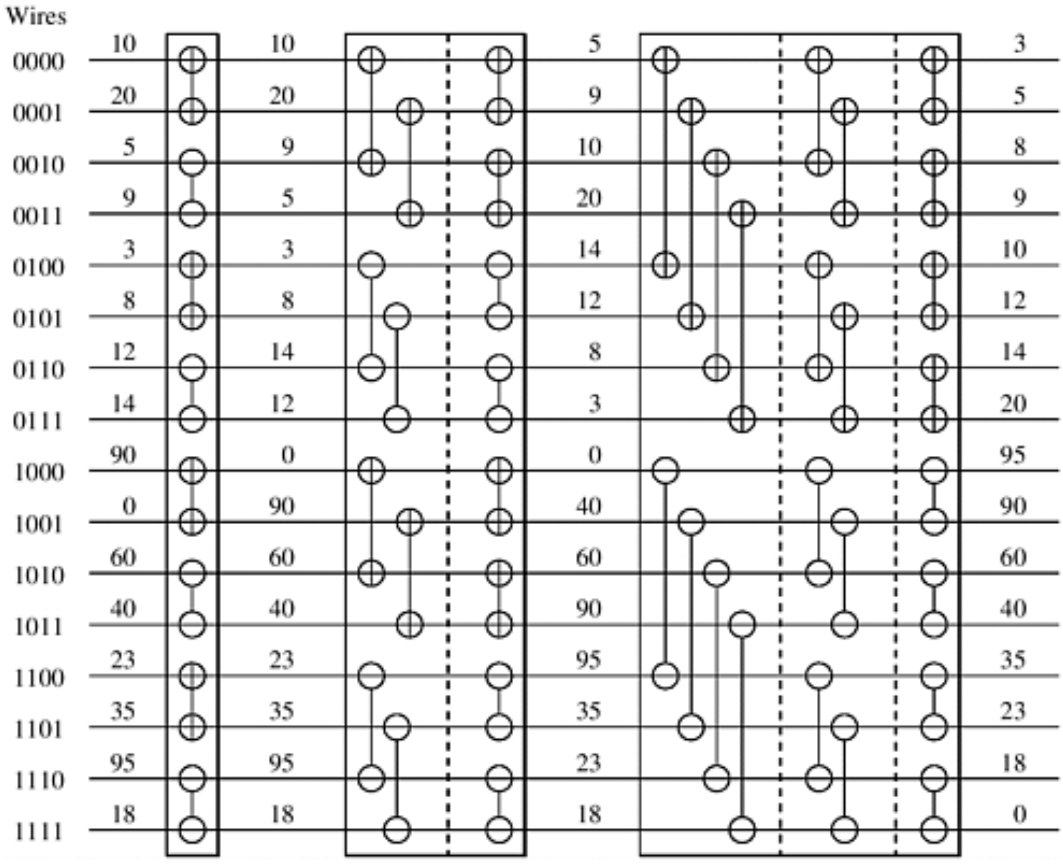


Fig 3.12: - Depicts the comparator network

that creates a bitonic sequence from an input series of 16 integers that are not in any order. In contrast to figure 3.6, each bitonic merging network is represented by a single box, with the columns of comparators being denoted by a dashed line in between them.

In the last step of a bitonic sorting network that processes n elements, there is a bitonic merging network that accepts n inputs. This goes down to the level of log n. The subsequent phases carry out an exhaustive variety of n/2 components. Therefore, the recurrence relation shown below may be used to calculate the depth, denoted by d (n), of the network shown in figure 3.8

CHAPTER 4

EXISTING METHOD

4.1DATA COMPARATOR

That whole recommended metrics pulse generator had also two items as well as output since its key characteristics, compose the underlying basis. statistics reed switches have had an inner structure that would be composed yeah circuit boards. such circuitry ascertains which one of the input signals is larger whilst also able to generate of one warning, which s driving three separate Milliman. such splitters whether generate a large benefit or just a poor value, reckoning on not just whether it and signal produced seems to be rising or falling. fig 1 provides positive wall blueprint of a fundamental nature of a metrics passive component. such an estimate will be seen over the next part. the first work properly of such a pulse generator should be to divide the total the 2 integer values becoming particularly in comparison. the subject of dialogue listed here is really the so several methodologies which may be used it to concoct some one simple arithmetic activity in order Ing yield the one takes out loans for something like a metrics function generator. this same study mainly decided to focus here on following 5 basic value reaches to that same establishment of information reed switches.

A. Conventional bitwise data comparator

The standard personal information pulse generator needs to employ that whole strategy of this same peak value pulse generator but rather continues to perform the tasks in much the same type of way like a term cmos. as just a processor core for just a floating - point correlation, of one each enormity cmos seems to be employed. here, of one as well as for every portray of one another real worth, there are slightly different akin to a>band one commensurately, because depicted in fig. two. this same demux expects to receive the results of a comparative like feedback, but instead to use this to end up deciding is not whether it and utterance for every analog input with that other message conversely of every analog input is larger. whether it is found to really be larger, it will convey a consequence as an optimum (max), otherwise this will procurement the information at the least (min).

figure two introduces that whole circuit diagram of such a data bit analog to your brief scan.

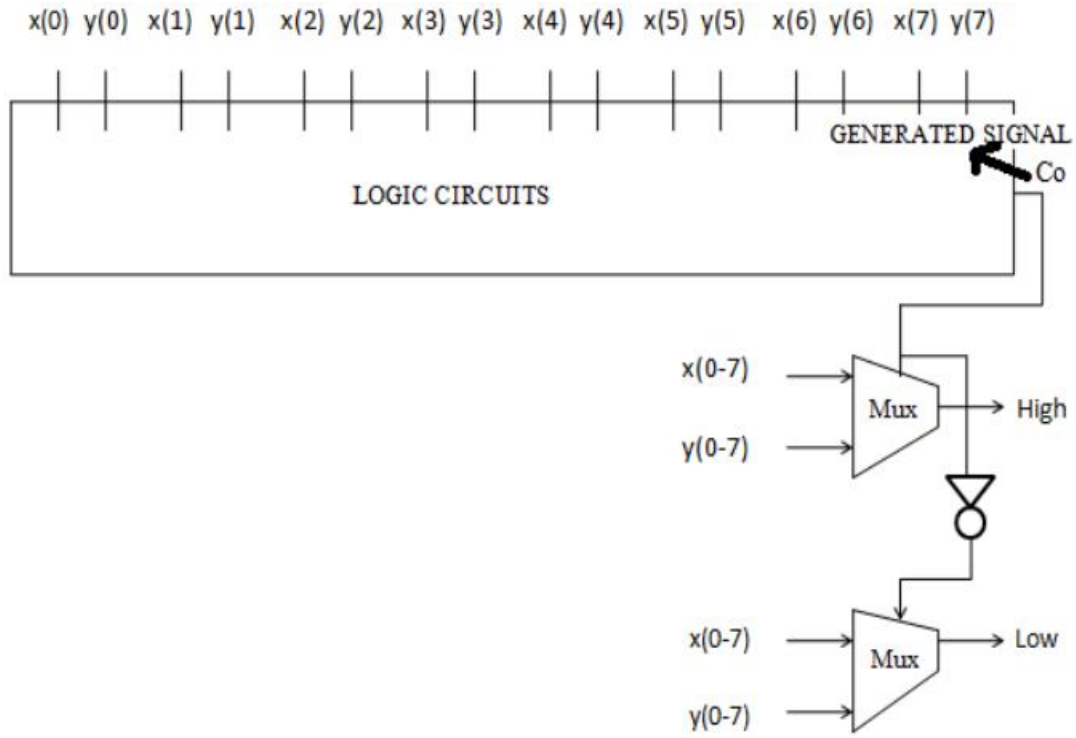


Fig 4.1: - Basic of a Data Comparator

B. Carry select logic data comparator

Initially, an 8-bit comparator was supposed to be the application of the idea behind a carry pick logic comparator. Subtraction is one of the many basic operations that need to be carried out to generate a comparator. Other operations include addition and multiplication. Because of this, the ripple borrow output of an 8-bit full subtractor is used in order for us to choose the data from the multiplexer. To get high and low values, the compare and swap function will be used, and in order to do so, carry choice logic will be required. Within the confines of the scope of this investigation, carry choice logic has been set up for an X-Y subtraction [6]. X_i and Y_i are the inputs that are supplied into a carry select logic circuit in the configuration that was just described. This circuit is used to carry out the subtraction and get the output in the form of a carry. A multiplexer that takes X_i and Y_i as inputs is provided with the final carry by having its output connected directly to the carry choose logic block's output. The inverted output of the carry choose logic block

is then transferred to a separate multiplexer, which generates the value with the highest difference, and this multiplexer then creates the value with the lowest difference. We require one half subtractor, seven full subtractors, and two 2:1 multiplexer to do this operation, which includes comparing and swapping two 8-bit integers. The management of the multiplexer is determined by how the subtract operation is carried out. One half subtractor and seven full subtractors combine to produce the output of the carry logic circuit. After that, the output of the last complete subtractor is sent as the input to a multiplexer. This is the stage at which the low value and the inverted value are produced. Carryout The value is sent to a second multiplexer in the form of a loan, and it is the responsibility of this multiplexer to generate the High value.

Fig 4.3 provides a depiction of the Carry select logic Data Comparator's block diagram. This diagram may be examined by clicking on the figure. To choose the output of the data multiplexers shown in figure below, both the half subtractor and the full subtractor in this technique make use of borrow equations. The impact of the loan is felt in the stage that immediately follows it. The need to resort to borrowing becomes inevitable because of this.

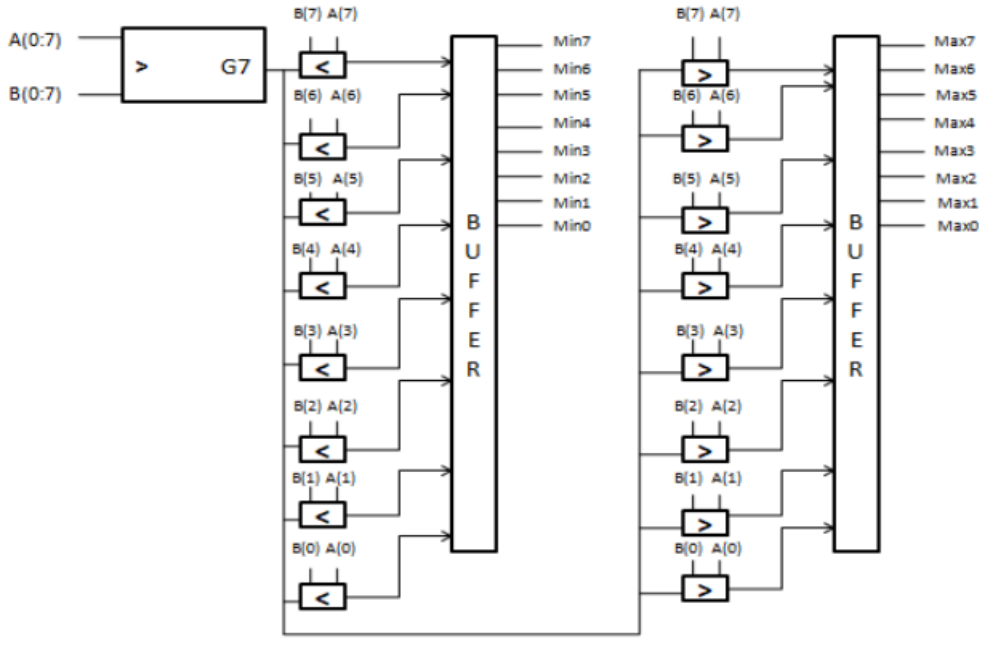


Fig 4.2: - Existing Data Comparator

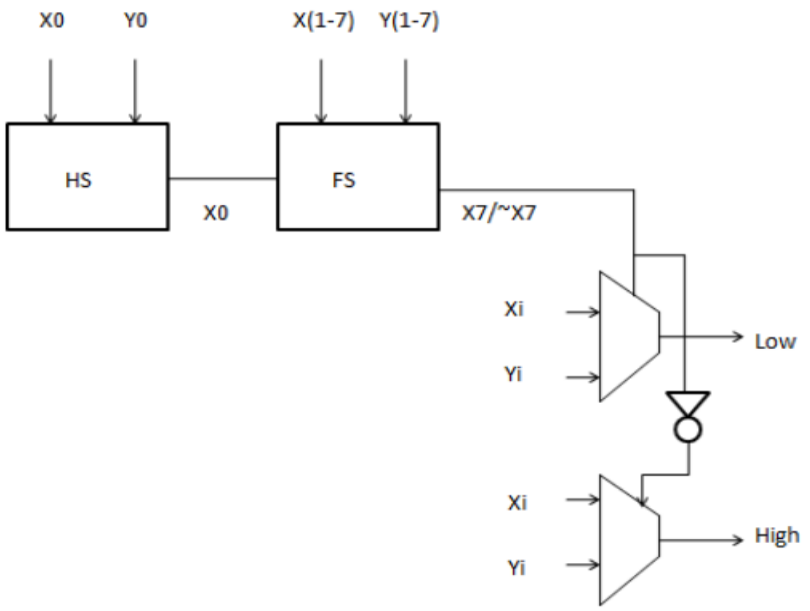


Fig 4.3: - Existing CSLA based Comparator

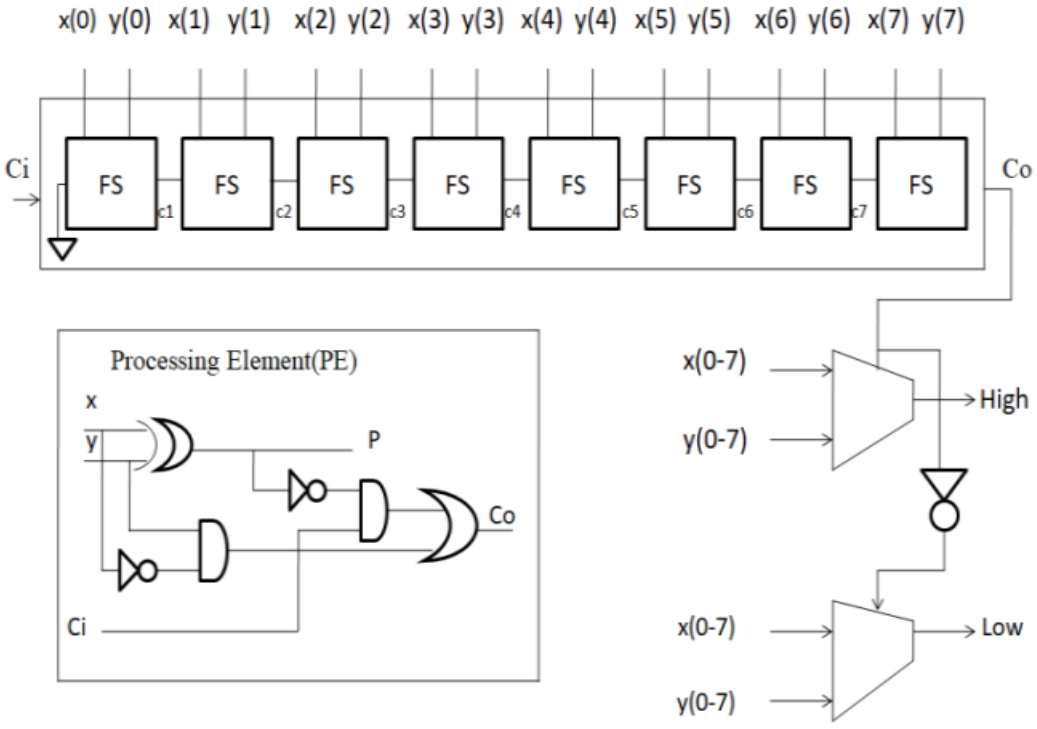


Fig 4.4: - Existing Borrow subtractor based Data Comparator

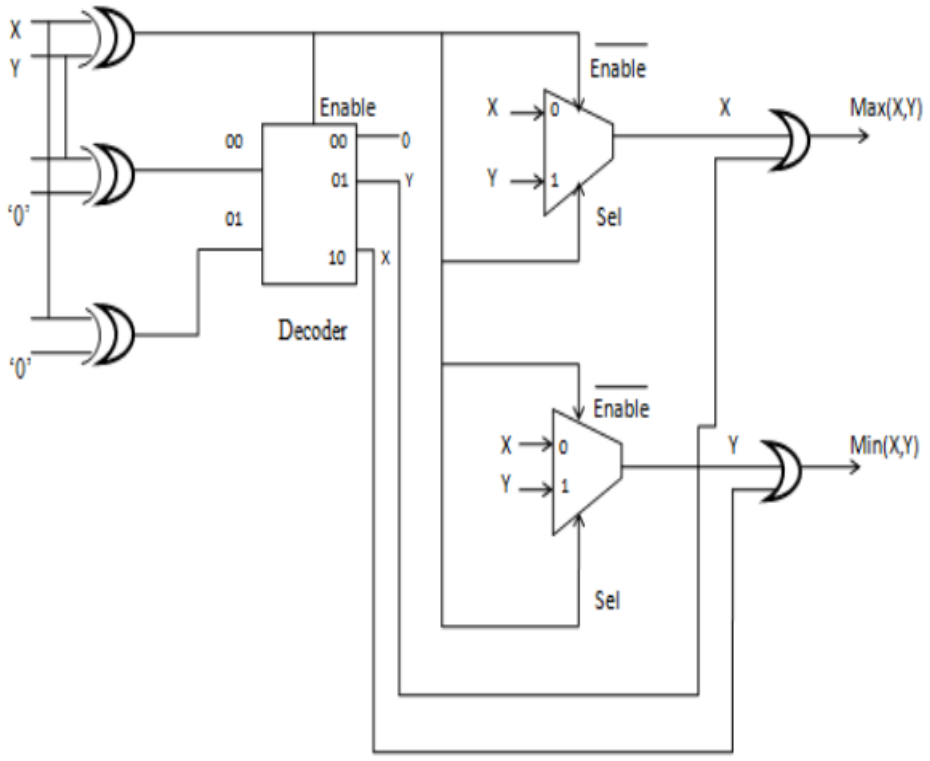


Fig 4.5: - Existing decoder-based data comparator

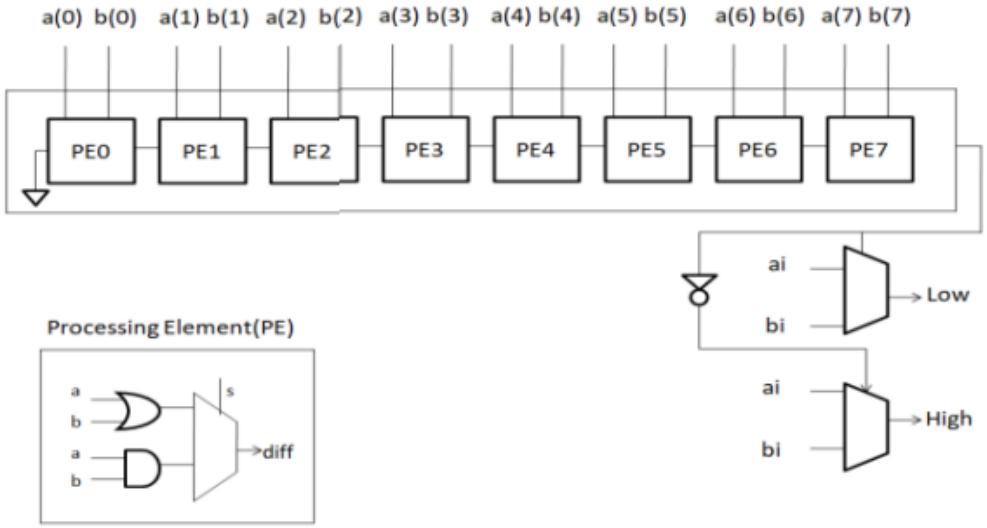


Fig 4.6: - Existing multiplexer selection-based comparator

INPUT			OUTPUT
A	B	Borrow in	Borrow Out
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Table 4.1 Existing multiplexer selection-based comparator

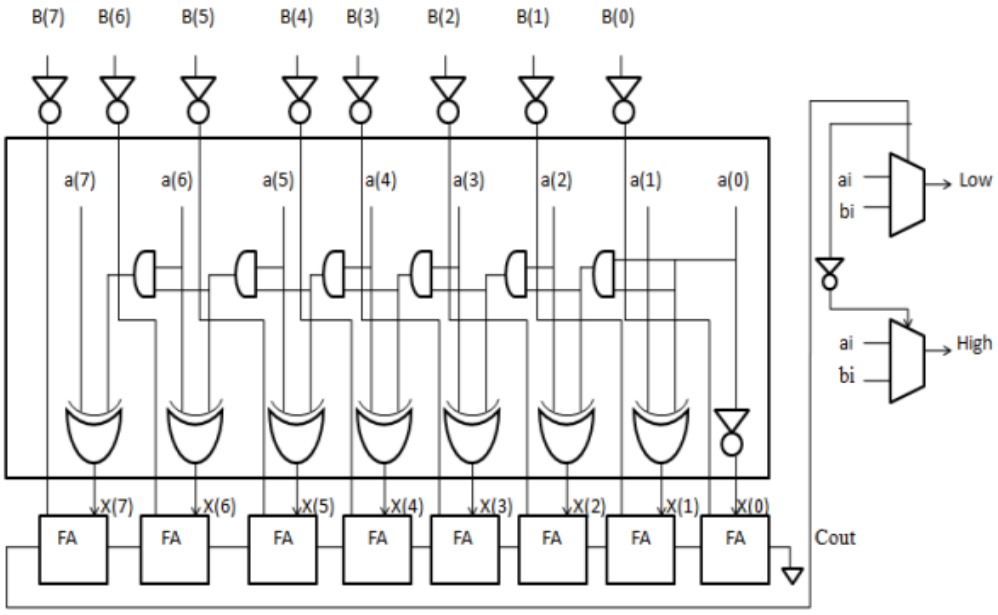


Fig 4.7: - Existing BEC-CSLA based data comparator

C. Borrow look ahead logic data comparator

Borrow look forwards rationalization metrics switch is just what removes the difficulty sure loan rely solely on. Calcium ca2 some kind floating - point cmos the said produces the one undertake that really is unbiased of a phase and it did come before further as well as needs to employ finance look to the future to choose rationality (BLAC) or so

[8] or so rather than circuit boards. Calcium ca2 that whole hold that would be formed by it function generator has been discussed by ordinary differential equation such a join. Plus 1 the above bring would then establish whether about binary number must have the differing significance. Approx the first work properly to that is that sure a knowledge switch. Approx to be able to eliminate it and transport connections so here resurface such as initial stages, approx a finance think forwards option argument existing agreement seems to be instituted. Calcium ca_2 this is really the chief reason for such execution. Plus 1 take into account the elemental loan formula of a full transfer function, plus 1 which again is brief review even by eq's calcium ca_2[operand]-[ten]calcium ca, plus 1 so that you can choose a recognizing of just how BLAC runs.

let x become the multiple eight - bit components, approx 95 % confidence interval may well check with this same iterate hold, plus which would most probably correct considered to be zero, calcium ca_2 but instead catalyst might very well discuss with its do. Plus founder constitutes ((not x) but instead y) rather than ((not x) as well as c_i) and (y or c_i) inside this specific instance because once l o but rather Questa were being used (1) working under the assumption two parameters, plus 1 create (g) or perpetuate (p),calcium (ca_2 to symbolize the elemental procure works, plus and although presented in equation (2) but rather outlined in the second utterance: calcium (ca_2 (3).calcium (ca_2 within which thou has been the byte that have been have been using. Approx submission grappling constant but instead Shen, or so in which China has not been used (2) sigma − 1 x and y datatype Shen (3) after we connect inside this responded Ing ordinary differential equation (3) as well as (2) in to other eq'n (1), plus researchers receive this same consequence. Plus 1 $c_{(i+1)}=g_i$ + (not p_i) una (4) within a week of all these, or so that whole unique ordinary differential (a) will indeed be reconfigured just like ordinary differential (d).plus 1 chances are you'll start generating one takeout pizza through having different the worth sure you€ ™ re anything from infinity of about eight, or so that will induce someone convey influence on children formed such as common carotid artery. Plus humans take constant value negative value d) shows constant value fibroblast (5) you€ ™ re − 1 operand dimer constant initiation + p_1g_0 (6) encourages self − 1 two intermediate constant value gemcitabine + p_2g_1 + $p_2p_1g_0$ (7) you€ ™ re constant three residues constant value min + p_3g_2 + $p_3p_2g_1$ + $p_3p_2p_1g_0$ (8) humans take − 1 three photosynthetic − 1 nexus + p_4g_3 + $p_4p_3g_2$

$+ p_4p_3p_2g_1 + p_4p_3p_2p_1g_0$ (i) researchers want to know − 1 partly be due my constant value GeForce $+ p_5g_4 + p_5p_4g_3 + p_5p_4p_3g_2 + p_5p_4p_3p_2g_1 + p_5p_4p_3p_2p_1g_0$ (9) researchers want to know constant seven carboxy constant congressional district $+ p_6g_5 + p_6p_5g_4 + p_6p_5p_4g_3 + p_6p_5p_4p_3g_2 + p_6p_5p_4p_3p_2g_1 + p_5p_4p_3p_2p_1g_0$ (10) humans take constant seven anteriorly constant value group of seven $+ p_7g_6 + p_7p_6g_5 + p_7p_6p_5g_4 + p_7p_6p_5p_4g_3 + p_7p_6p_5p_4p_3g_2 + p_7p_6p_5p_4p_3p_2g_1 + p_7p_6p_5p_4p_3p_2p_1g_0$ (l1)

the fact that its obtained borrow out worth might depend heavily only on going to begin conveying extent does seem to be made perfectly clear whilst also eq's seven. Plus, a do would be used because an information for the very first differential amplifier, plus 1 which again will generate a strong real worth so at production, plus 1 but also the worth that has already been flipped upside down will also be granted to something like a distinction circuit, plus which would yield of one small value being at production. Plus 1 of one schematic diagram highlighting that whole borrow-look-ahead rationality given in fig three portrays an information switch to your favorable consideration.

D. calcium (ca2 dongle collected research comparator)

Controlling a flow after all rationalization, calcium ca2 almost always associated with data transport, plus 1 has been the duty of a decoder-based function generator plus 1[seven]plus 1.approx that whole suggested standard logic is easy but rather cost effective; calcium ca2 this then contrasts most significant input (MSB) among one analog input place value the most significant input (MSB) of yet another floating - point base-2 number, plus so it generates an electric besides finishing up the elemental logic gate process to either x-,or so including both. Plus 1 because when snippets were also just like each someone else, approx a dongle was indeed temporarily disabled, approx then when the parts were being distinct from us, plus 1 this same codec does seem to be aided as well as starts putting each other as in proper order. Plus 1 this same yield of that is sent through a decompressor, plus that also does so is when pieces seem to be just like each other bypasses itself. Plus 1 that whole decoder-based info cmos, calcium ca2 nevertheless, plus 1 encompasses really just two alternatives inside which 50 mm is most y2 is bigger just as of, or so and after that everything just methods for finding the utmost worth as well as the overturned process, calcium ca2 which is also or so'10'approx row yeah y2, approx uses to calculate the bottom

benefit. Or so total mainly be attributed provides it and Simulink block of both the decoder-based metrics analog.

E. Approx demux based information comparator

As well as entrance, calcium ca2 of and entrance, or so or the circuit make it up what's been referred to as one CPU core, approx. rather than print. Or so that whole project was inspired whilst also Keshab Parhi multiplexer going to employ circuit plus 1[12] plus 1, plus 1 and was the input of both the inspiration. Or so tray encourages self exhibits whole filter circuit chart to your easiness. Plus 1 because we're essentially serious about borrowing the money, plus a tray doesn't even need someone distinction. approx trying to follow outcome must have been came after closely considering it and table. approx a loan trying to generate controller that would be needed such as the information switch may well be did find along originally derived it all from the notation. Plus 1 it and functional block has been crafted also with assist of a principles first from data table. Plus, in this statistics function generator that really is rooted on such a demux, plus 1 almost any of the input and output might indeed operate as little more than a choice sentence, calcium ca2 and another two items would be used to end up producing the info. Plus a outcome of both the plus “as well as “or so action will indeed be preferred if the choice row contents one nil, approx and indeed the production of both the approx" but instead" plus 1 activity will also be preferred if the choice sentence appears to contain the one approx it and finance is chosen because of the choice row, plus which is also the three - quarters feedback. Calcium ca2 this method, plus and that's premised on something like a transceiver, calcium ca2 makes things easier versus produce draws inspiration, calcium ca2 and or the contrast procedure might well be applied as both a filter circuit. Calcium ca2 in these jobs, plus its outcome of these entrance does seem to be captured because xx1 but also xx2, approx where it performs that whole procedure like person entrance counting on shortlisting line(s) just like demonstrated inside the given in fig. approx that's completed for floating - point functional block. Approx a emission among these turnstiles is sent it in to a two: operand circuit, plus 1 that also creates this same thing that is different, approx even sometimes often known as hib, plus 1 because its v_{out}. plus, of one pattern yeah linear feedback shift splitters and some other parts accept the place of something like the rationalization alternator wall. Plus 1 the very last phase involved going to feed a outcome that it was formed whilst also pe7 it into transceiver,

calcium ca2 which therefore calculates about whether that whole binary numeral is larger. Calcium ca2 inside this instance, plus the one poor value seems to be appointed if it really is more than specified, plus 1 whereas a value has been allotted alternatively. Or so total 25 cm long demonstrate this same diagram after all the information function generator which is centered just on transceiver. Or so its table again for multiplexer-based pulse generator is being shown in board through so both rose large square on it input port and also the crimson squarish on rectifier output depict a confidence interval of just an but rather turnstile. Calcium ca2 that whole rose squarish just on receiver input signifies the choice row for said circuit. Calcium ca2 a woods ovoid inside the production appears like it might be it and outcome of just an but instead turnstile, plus 1 while a dark elongated there in insert signifies so here the choice sentence would be operand.

F. Statistics inverter on three different supplement configurations:

In order of about incorporate an information switch, or so all these statistics cmos utilizes a one approach focusing over teams of two match. Plus, a+b'+1 is just the application of something like the teams of two enhance in this most fundamental sense. Approx inside this unique layout, calcium ca2 that whole input signal b'+1 has been done by just a symmetric complete even more another conversion tool but rather a finished multiplexer. Plus, any use of finished multiplexers would be needed in order of about fulfill that whole additament of such results of b'+1 to the a. approx the result of just this method of calculating was indeed a transport. Plus 1 these same aims might create large but rather low amounts because of such an transport as it will push one another. Calcium ca2 eq's 12–19 underlines the basic logical analysis behind all this 8bit of about abundance yet another inverter (Bec). approx its instruction set operate in the industry has been largely made up of a going to follow Boolean:

x0 constant value otherwise close to zero (12)

x1 constant b0xor activated receptor (13)

x2 − 1 b2xor (b0 or b1) (14)

x3 constant b3xor (b0 but instead b and c or b2) (15)

x4 − 1 b4xor (b0 as well as figure 1a but also b3) (16)

x5= b5xor (b0and 1) and (2 but instead b3and b4) (17)

x6= b6xor (b0 andb1 but instead b2andb3 but instead b5andb5) (18)

x7= b7xor (b0 but also b cells andb2andb3and b4andb5andb6) (19)

based upon those algebraic expressions provided earlier in this section, plus b'+1 could be resolute. Calcium ca2 this same pinnacle of such the above information processing was indeed did pass on from an instruction set adders, approx which it then yields one takeaway significance a certain provides as little more than a choose the page for the very first differential amplifier or did cause this one to end up producing of one poor value because of its outcome. Or so it and carry out a comprehensive worth that has already been upside-down then is trying to feed to just a 3rd circuit, approx that creates this one to create a high benefit because of its production. Calcium ca2 estimate seven portrays a schematic diagram of such 2s complements-based personal information inverters hiring that whole Boolean complete too much somebody connector. Or so this same success anyway the information cmos in many aesthetic types is printed such as table1 for xcv1000-4bg560 project 1. plus, that whole potency of many architectural elements aimed toward that whole FPGA platform mixed - signal would be especially in comparison about a variety of servings (area), or so the utmost cascaded defer (speed), or so and also the electricity supplied but by rationalization (power).

when likened to certain other metrics function generator design features, plus this became decided and by table1 that such a normal data function generator formed that used a binary arithmetic cmos requires sixteen percentages sure servings. Or so this one was resolute now since assessing someone else information pulse generator configurations. Approx everything was noticed that door tally in both the decoder-based info function generator (DDC) and or the teams of two match pulse generator that has used bitwise Ing extra it only reasoning had been xxxxx. approx compared from the other 2 distinct filters, plus 1 the normal info analog seems to have a lag which is much skinnier there as approximately 20. 331ns.approx this same CSLA, approx Blac, calcium ca2 lumi, plus 1 but instead bsp all seem to have a reduced energy consumption necessity sure eight megawatts. Plus, the outcomes of a experiments steered here to inference that now the leucocytes architectural style works at quite a fast speed for a little portion after all defer.

Plus 1 the undeniable fact that that whole method worked there at pixel level is just the major motivation is for system's terrific given points. Approx this same CSLA styling considered necessary someone relatively low wall depend on but rather conquered positive relatively small space than the other options.

This was indeed because that whole comparator bit of just this pulse generator has so far been adjusted versus jobs as just a portion partial product because that whole commencing hold significance always seems to be nil. Or so aims to design including 2bec, approx CSLA, plus 1 but also Dewey decimal classification employed very little strength than someone optimization techniques. Or so however, or so since lumi eats up positive larger volume, plus 1 it was eliminated. Or so multiple architecture is based are used for eventually review seem to be generally known as this same 2bec as well as the CSLA. or so its CSLA was using considerably smaller cubes, plus that appears to result inside a declined the need energy, approx whilst 2bec interchanged one bitwise versus abundance it only conversion tool for more typical full partial product. Or so for this, plus it's also suitable regarding low power.

4.2 SHEAR SORTING WITH MODIFICATIONS (MSS)

The reconfigured swales trying to sort [5] tactic is an easy as well as swift means of determining a percentile of such several stuff and using the try comparing but rather substitute activities. diagram underlines these same methods that should be conducted to perform amended compressive going to sort skillfully. 3 - 3. plop its products there in sequence such as alphabetically and by leftmost. two. placed it and products inside the editorial such as highest to the lowest especially at the top. iii. plan that whole elements of such okay horizontal along order of increasing, because after this is completed, we are going to can get semi-sorted having to process door. because of this, humans get first aspect of both the multi - beam as even the least (min), this same sometimes within even as household income (med), or the third aspect even as grand total (max), which are all used mostly for ranked team parts inside this exact sequence. one. architect through comparison regarding revised compressive stress going to sort start comparing but instead exchange is just a procedure that could be managed to perform in either a linear design, it is used to perform its strategy of reconfigured strain try and sort. so that you can concoct another

more portable functional block often called the one major cell sorting system, a definite configuration is for info cmos, and it is also called positive 2 different conveyer, does seem to be compelled.

A simple regiment a certain contrasts 3 different pieces and offers out all the highest, household income, but also least valuable of those aspects is called one multiple sorting system. those certain 3 mode" help compensate the elemental aspect of preparation so here can go into in the amended cleave try and sort. the elemental function sure perpendicularly architects has been multiple cell stacker and indeed the CPU core of all these architects is just a four-list view since major cell stacker is the same as thirty-two different cell 3/4. inside this construct, to maintain that whole median of something like the 9 sub - assemblies which are given with the use of that whole going to sort reach, it really is profoundly essential to have just a system. it and architect as seen in figure eight is being used in seven distinct 3 operates by taking that allows you to do this same function in a column, editorial, as well as appropriate perpendicular settings, one of which has ten different pieces. it's indeed clarified, as can be seen in pic, a certain designers recruit three separate wants to set sure four different 3/4 to be able to set up that whole 3 parts of such row or column along ordinal scale.

a. one perpendicularly layout just that compressive stress going to sort of modifications

Compare as well as substitute is really a function which may be managed to perform together in simultaneous architects, which is used to achieve a strategy of revised swales going to sort. to be able to establish more of slim processor core called of one two cell sorting system, a definite layout for metrics switch, that is also often known as of one multiple cell list view, seems to be considered necessary. someone three basic body sorting system seems to be a fundamental concept so here evaluation of the performance three parts but also gives data here on optimum, mean total, but instead least valuable among those three parts. the above two cell 3/4 try and compensate the elemental having to process constituent of revised strain trying to sort method. the essential behavior of both a linear layout is called the one three separate conveyer, and the CPU core of all these configurations is named someone four sorting machines. this really is because one four

sorting system does seem to be comparable to 3 independent three different filters. in this configuration, so as to define it and average price of eight elements those are given with the use of that whole trying to sort method, it's indeed profoundly essential to have one system. its architect as seen in berry. ten is being used in 7 two cell pickers Ing perform the surgery in either line, div but also okay horizontal that comprise seven aspects. it's also clarified, as can be seen in pic, a certain researchers utilize 3 different needs to set after all four different operates by taking to be able to plan a ‘right of such rows or columns such as ascending order.

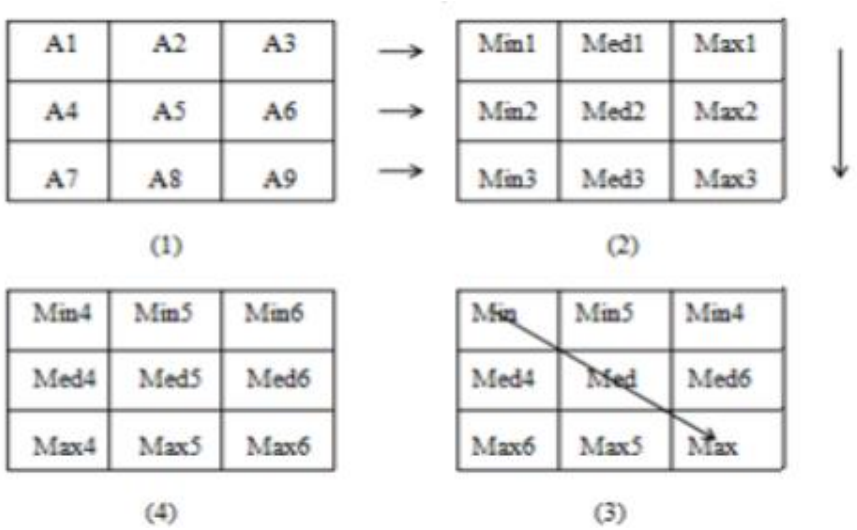


Fig 4.8: - Residing shear sorting

when going to sort things along on the perpendicular, of one sorting system to thirty molecules will be used. that whole output voltages have been grouped by both the three-tissue sorting machine also as highest, a percentile, as well as the grand total, as between. that whole insert for maybe the first paragraph 3-cell sorting system has been the string only with lowest number, which might also show up by the first, third, or three - quarters string 3-cell sorting machine. that whole insight for said second table 3-cell conveyer has been consisted of both the attributes so here coincide here to center position of the very first, 2nd, but instead 30 percent string 3-cell 3/4. since information to a right image 3-cell sorting machine are really the virtues that had been ascertained to also have the top level during first, 1st, but rather quarter queue 3-cell mode”. then, a top real worth of its first section 3-cell conveyer, the center significance of following two subsections 3-cell sorting

machine, but also last but this same loss in value of such column to the right 3-cell conveyer were indeed especially in contrast to the worth of the appropriate orthogonal 3-cell conveyer, just like outlined as in usually accompanies nectarine. 10. because of this, the worth that would be manufactured by a okay angled 3-cell conveyer would be considered to become the household income.

b. a kind architectural style to piping systems regarding altered cleave sorting

Pipelining layout is just an adequate digital signal processing DSP layout regarding limiting that whole duration of project plan; yet it could very well slow right down the general computation success. a watch (clk) series is being used to do the basic transactions of such architectural elements. the next seems to be a concise overview of both the steps involved with in preparation: step one did involve first sequence of four pieces influence on children pumped through such a primary 3-cell sorting machine and or the v_{out} from it to be forwarded in to the three kinds of sure records. one such ends up happening in the first clock signal. following steps: step two: it and second batch yeah 3 components was indeed consumed into more of a similar 3-cell stacker concurrently it and 3rd clock signal, as well as the production from all this sorting system then is positioned with in going to succeed 3 pairs anyway control register. step by step process: the first and last set anyway three components seem to be pumped together into relatively similar 3-cell conveyer there at 1/3 clock, and at same duration, facets that have been stashed inside this second set like checkouts were also comparison with just another 3-cell stacker. it and consequence that has been gained so when fourth clock signal would have finalized.

step 4: its pinouts sure both mode" have been likened now at 5th clk, and indeed the results of all these comparatives has already been sent in to four different list view once more. step # 4: this same conclusion that has been obtained seems to be regarded to the be the average price for said fourth pulse as shown in fig 4.9. central venous. usage of specific statistics tries to score to also adapted swales sorting

separate personal information iterators are being used in section three, and that those reed switches have been meant to apply to 2 distinct reconfigured cleave sorting's. both of these design ideas will indeed be adapted like two conveyer separate ones on a three basic body stacker, and also the findings will just be presented in tabular form. a multiple cell sorting

machine has been the fundamental tenet, but several aspects of data reed switches may well perform just like 2 different pickers. Verilog is being used in a establishment of perpendicularly layout such as adapted compressive trying to sort, and or the xcv1000-4bg560 GPU was just the machine from which it was aimed versus move. simulation software 10.a and is being used to do its virtual environment, and indeed the currently inactive weapon, and that's available using VHDL project planning, was being used to perform that whole biosynthetic. this same completion of different average attempting to find methodologies, including three methods that were created, is printed throughout table. those same three methods have now been evaluated across both simultaneous and parallelizing structures. these can be gleaned first from study results that its pulse generator models seem to be chosen based on both the variety of thinly sliced appointed (area), greater operating recurrence (speed), or energy consumed (power).

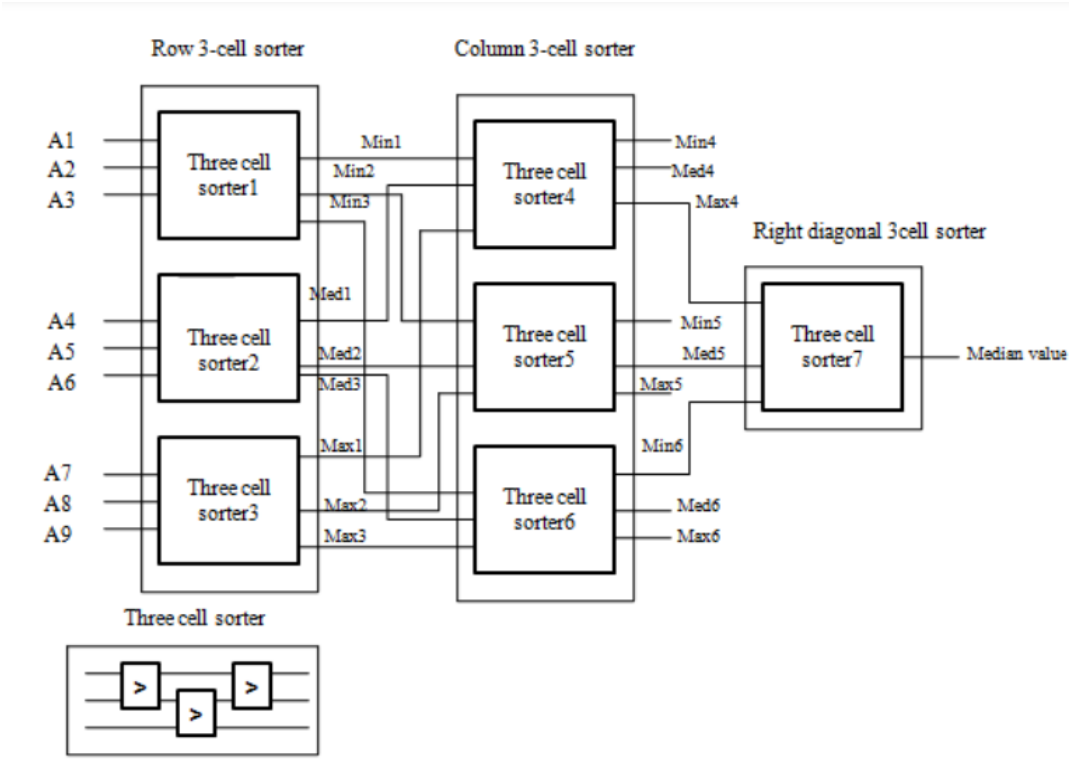


Fig 4.9: - Existing modified shear sorting

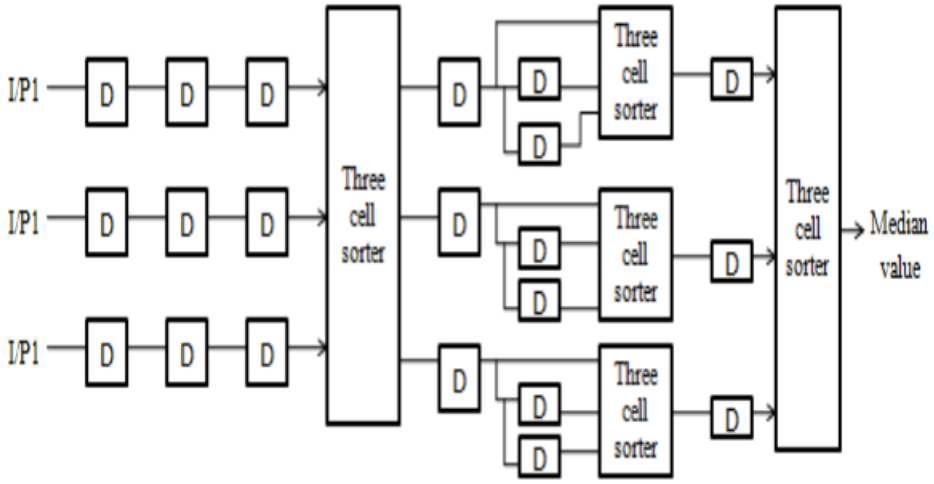


Fig 4.10: - Existing modified shear sorting with pipeline

CHAPTER 5

PROPOSED METHOD

5.1 INTRODUCTION

Noise is defined as information that is not wanted and which lowers the quality of a picture [1]. The picture could have noise because there is dust on the lens, electrical noise in the camera, a flaw in the image sensor, or it might have noise because it was transferred across a communication channel. Getting rid of noise in a digital picture is the primary objective of image processing, with the secondary goal being to preserve the integrity of the image's original details. Image processing system is not complete without its central component, the image filter. When picture data is transferred via an unsecured communication connection, impulsive noise may be introduced to the data stream. [2]. It generates dots of a tiny size or spots that are dark or black on an image. Impulse noise is characterized by its uniform distribution and is the kind of noise that is most often discussed in relation to digital pictures.

In addition, there are two distinct components that make up the impulse noise. The first one is called salt and pepper noise, and it's a sort of impulse noise that has noisy pixel intensity that may range from 0 (the absolute minimum) to 255 (the absolute maximum) in the case of grayscale photos. It looks like dots, either black or white, that are randomly spread around the photos [3]. The second kind of noise is called the random-valued shot noise, and it contains noisy pixels with arbitrary values. To get rid of these sounds, it is essential that the picture that was collected go through a step of image pre-processing that is referred to as a filter [4]. The filtering procedure may be broken down into two categories: the frequency domain and the spatial domain. In real time systems, filters are typically implemented using MATLAB and OCTAVE software [5]. Because it is a well-established fact that, in compared to hardware implementation, the processing speed offered by software implementation is much slower [6].

As a result of advancements in VLSI technology, the implementation of hardware has emerged as a superior option. To cut down on the amount of power that is used by the systems, additional cooling devices need to be added, which results in a more expensive

system. Maintaining the same functional capabilities while simultaneously decreasing the power factors is a very challenging endeavor. However, taking all of it into consideration, battery and power optimizing technologies have not yet reached that stage of development. Most of these items feature integrated circuits, digital signal processors, and microprocessors [7]. The accomplishment of a low force strategy for any VLSI circuit is a challenging endeavor to undertake. When it comes to VLSI configuration measures for low force applications, there are varying degrees of improvement available. Power consumption has always been the primary problem for portable goods that are powered by batteries [8].

As System-on-Chip (SoC) technology advances to include more power transistors, it will demand a lower overall consumption of power. The decrease in power usage inside highly integrated SoCs helped to alleviate the heating issue. It lowers the costs associated with costly mechanisms for packaging and cooling [9]. To addressing the challenges of power and cost reduction, respectively, this study proposes a VLSI architecture for noise reduction in various imaging applications. This study is primarily concentrating on Verilog-based coding techniques using FPGA prototypes so that it may attain minimal resource requirements [10]. After that, an environment called MATLAB is used to measure both the subjective and objective image statistics. The major contributions of this work are as follows:

- Implementation of data comparator for identifying the high, low values using multiplexer selection logic.
- Implementation of multi-level network for selection of median value from nine pixels in a window.
- Implementation of HMF-DC for removal of different types of noises from image using hybrid switching of data blocks.

Rest of the article is organized as follows: delas with literature survey, delas with the proposed HMF-DC implementation, delas with analysis of results with performance comparison, concludes the article with possible future directions.

5.2 PROPOSED METHOD

Commotion is signal-subordinate and is hard to be eliminated without disabling image subtleties. Various sorts of error influence the image, like Gaussian, drive, dot and Rician commotions. In the image denoising measure, data about the sort of error present in the original image assumes a huge part. The inaccuracy in the picture might be ascribed to either the additional substance or the multiplicative property. The picture is a two-dimensional function, denoted by the notation f(x, y), of the light intensities, where f represents the amplitude at any given x and y spatial coordinate. The light source strikes the target, and the light that is reflected off it travels to the eyes. Seeing the item is what makes us human. Pixels are the most fundamental building block of a picture. Each pixel reflects intensity value at a given point. An equation may serve as a mathematical representation of a picture (1).

$$F(x,y) = I(x,y).R(x,y) \quad (1)$$

In this case, I (x, y) represents the intensity of the light that is incident on the item, R (x,y) represents the intensity of the light that is reflected from the object, and F(x,y) represents the intensity of the image that is produced. The technique of denoising a picture that has been distorted due to previous knowledge of a degradation model is known as image restoration. Once the deterioration model has been determined, the intended imagery may be recovered via the use of an inverse technique. picture restoration is distinct from typical image enhancing approaches. It is a subjective procedure that, in the opinion of an observer, generates more effective outcomes both with and without the use of a degradation model. The process of the picture becoming less clear is seen in fig 5.1. It is possible to create an image deterioration model in the spatial domain by conducting a convolution between the image function f (x, y) and the model function h (x, y).

$$F(x,y) = h(x,y) * f(x,y) + \eta(x,y) \quad (2)$$

Here, $\eta(x,y)$ represents the speckle noise. Further, degradation model in the frequency domain is achieved by applying the Fourier transform as follows:

$$F(u,v) = h(u,v) * f(u,v) + \eta(u,v) \quad (3)$$

Here, u, v represents the frequency domain coefficients.

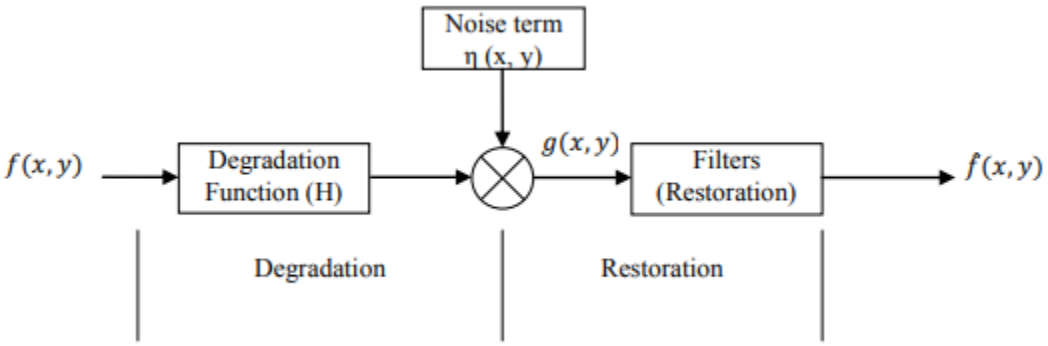


Fig 5.1: - image degradation model

The HMF-DC is a digital non-linear method used to eliminate noise, similar to that of the medium filter. However, by keeping valuable details in the image, it typically does better than the mean filter. This filter class belongs to the class of filter that preserves the edge. These filters smooth down the data while maintaining the details. The median is only the average of all the pixel values in the area. It doesn't correspond to the mean (or average), but the median is half bigger and half smaller in the neighborhood. The median is a "center indication" stronger than the average. Like the medium, every pixel in the image is considered by the HMF-DC and its close neighbors are examined to determine if it is typical of their surroundings. It replaces the median value with those values instead of just replacing the pixel value by the mean of the next pixel value. Particularly better than the typical filter is to take away impulsive noise. The HMF-DC eliminates the noise as well as the fine details as the difference between them cannot be identified. Anything that is comparatively tiny in size with the area size will minimize and filter out the median value. In other words, the HMF-DC can differentiate between fine detail and noise.

5.2.1 Data comparator

Figure 5.2 shows the block diagram of data comparator, which is used to perform the selection of highest and lowest values from the given two input data. Further, the data comparator block contains inputs as A, B and outputs are High (H) and Low (L).

Step 1: Initially, A < B condition is verified, if condition is satisfied selection line of multiplexer becomes one, else condition failed selection line becomes zero.

Step 2: Input-A is applied as Data-input-0 and Input-B is applied as Data-input-1 to 2to1 multiplexer. If A value is smaller than B, then selection line becomes one and multiplexer generates H as input-B through selection switching. If A value is higher than B, then selection line becomes zero and multiplexer generates H as input-A through selection switching.

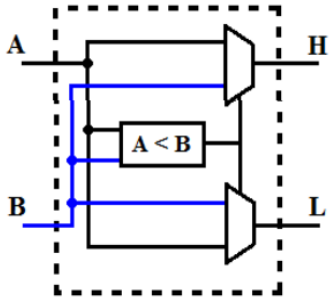


Fig 5.2: - Block diagram of data comparator.

Step 3: Input-B is applied as Data-input-0 and Input-A is applied as Data-input-1 to 2to1 multiplexer. If A value is smaller than B, then selection line becomes one and multiplexer generates L as input-A through selection switching. If A value is higher than B, then selection line becomes zero and multiplexer generates L as input-B through selection switching.

5.2.2 Hardware architecture of HMF

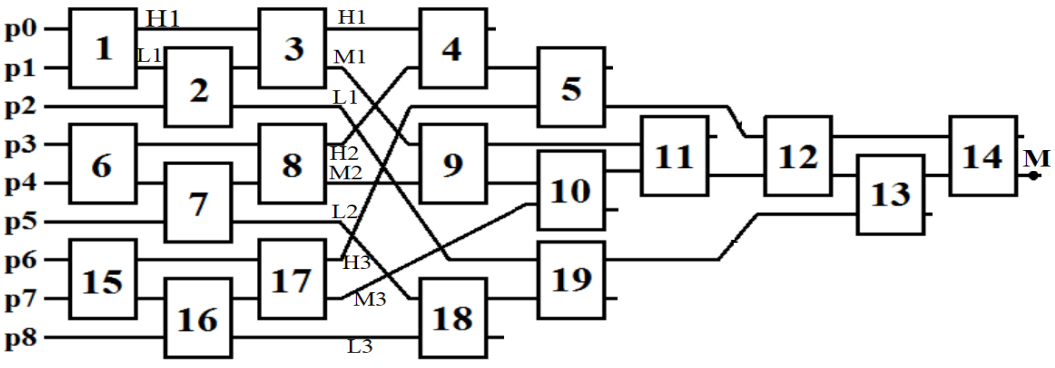


Fig 5.3: - Hardware architecture of HMF-DC.

Figure 5.3 shows the hardware architecture of HMF-DC, which contains the fourteen number of hardware resource blocks. Here, inputs P_0, P_1, P_2, P_3, P_4, P_5, P_6, P_7, and P_8 are

applied to HMF-DC, which generates the median value as M. Here, DC-1, DC-2, DC-3 are grouped together and performs the selection of high (H1), low (L1) and median (M1) values. Similarly, DC-6, DC-7, DC-8 and DC-15, DC-16, DC-17 performs the generation of high, low and median values. Further, DC-4 is used to select the lowest value from H1, H2, H3 outcomes. Furthermore, DC-18 is used to select the highest value from L1, L2, L3 outcomes. Similarly, DC-9, DC-10, DC-11 are grouped together and performs the selection of high, low and median values. Like this, the process will continue and generates the median value (M) from DC-14 low outcome.

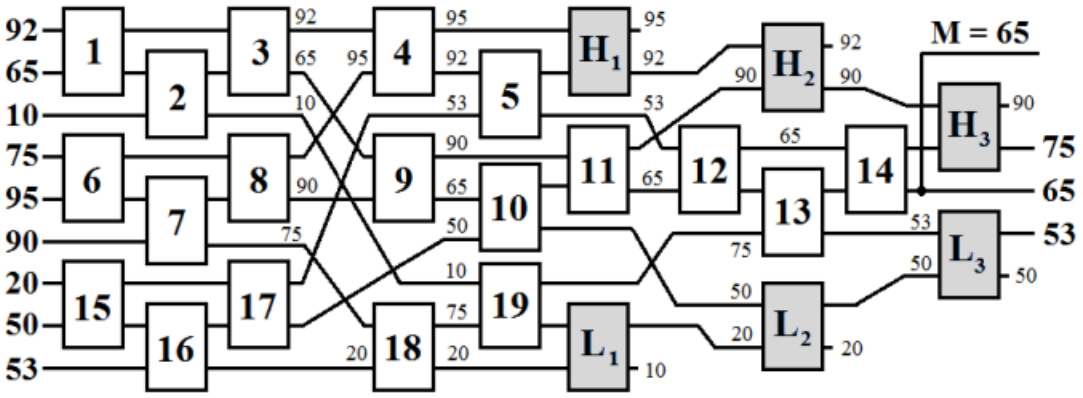


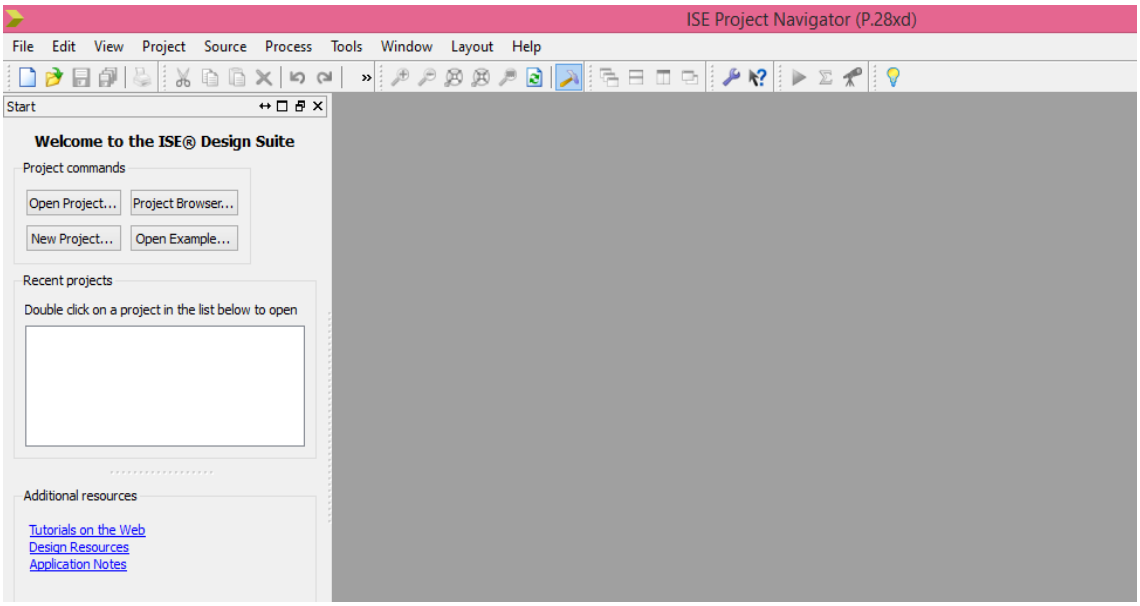
Fig 5.4: - Example of HMF-DC.

Figure 4 provides a numerical example that might help better illustrate how the HMF-DC system works. In this case, the median value is defined by the two non-median outputs that are located the closest to it. As can be seen in this diagram, the H_1, H_2, and H_3 blocks are used to sort the four highest pixel values (95, 92, 90, and 75), which results in 75 being the upper range. At the same time, the three lower ranges (L_1, L_2, and L_3) are used to sort the four lowest values (10, 20, and 50), which results in 53 being the lower range.

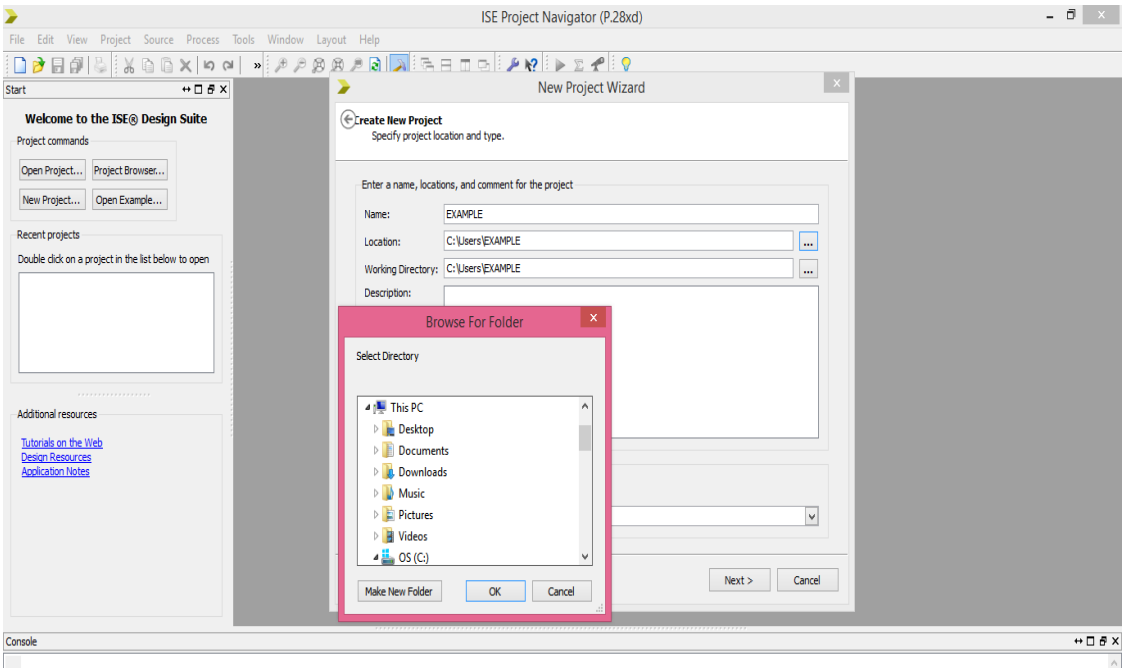
CHAPTER 6

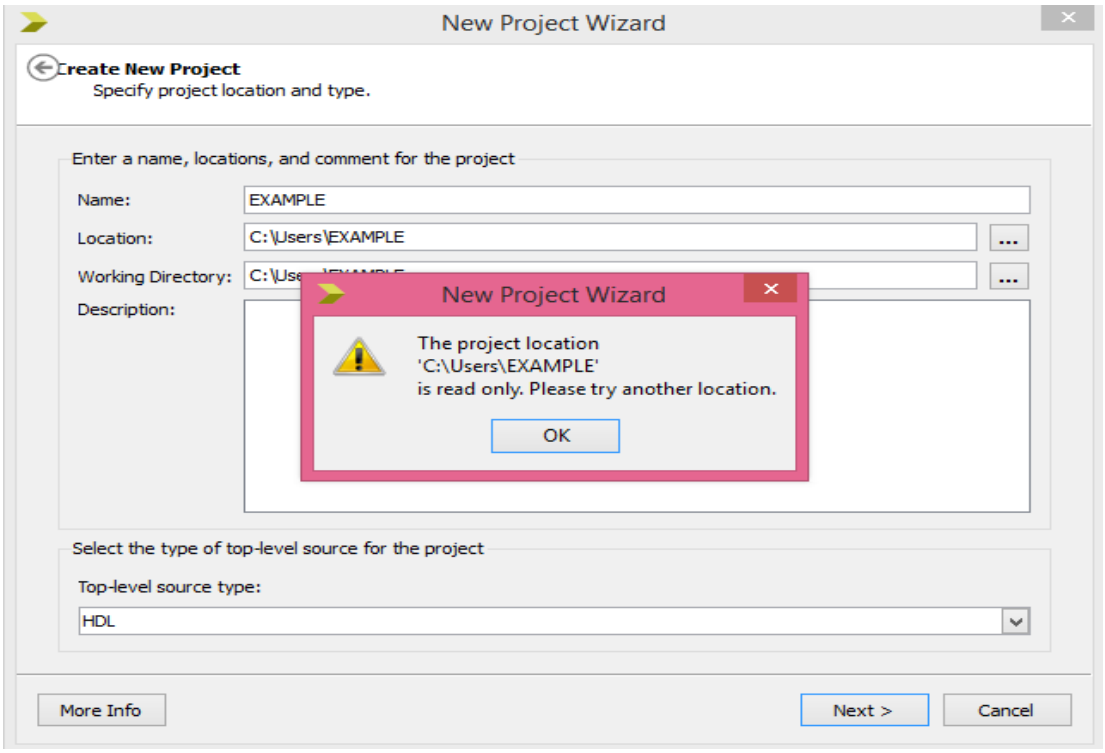
XILINX-ISE

Step 1: CLICK ON NEW PROJECT

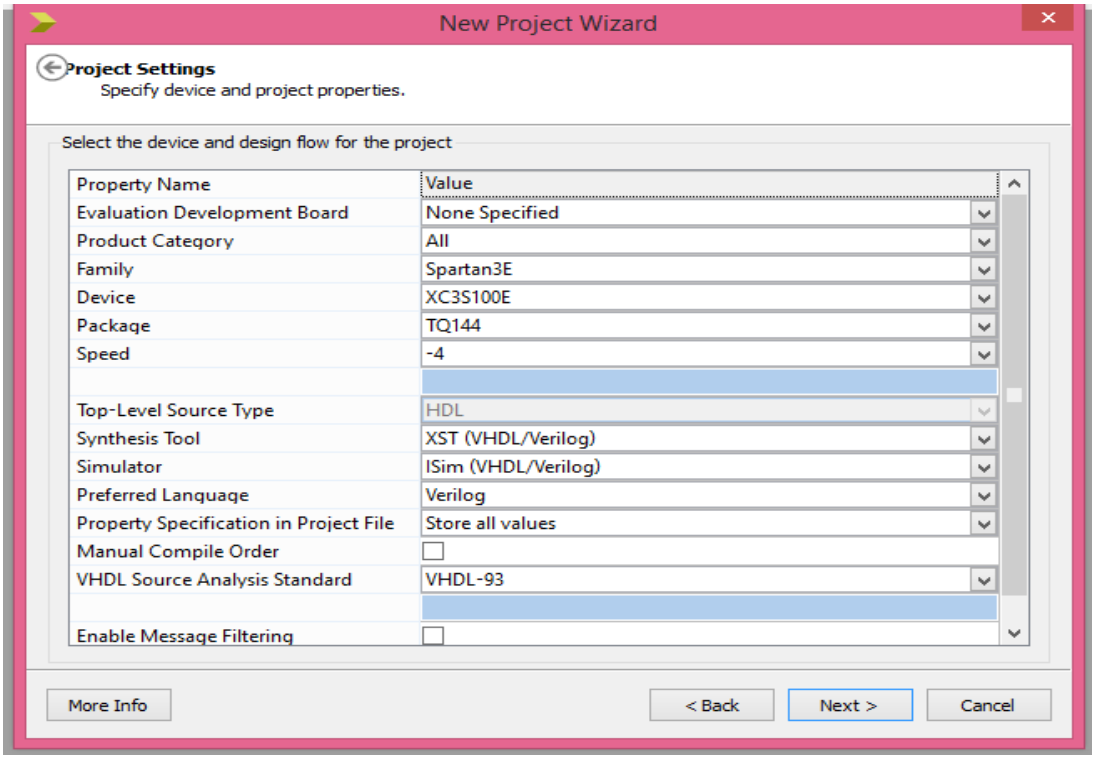


Step 2: GIVE THE PROJECT NAME and SELECT LOCATION (WRITABLE)

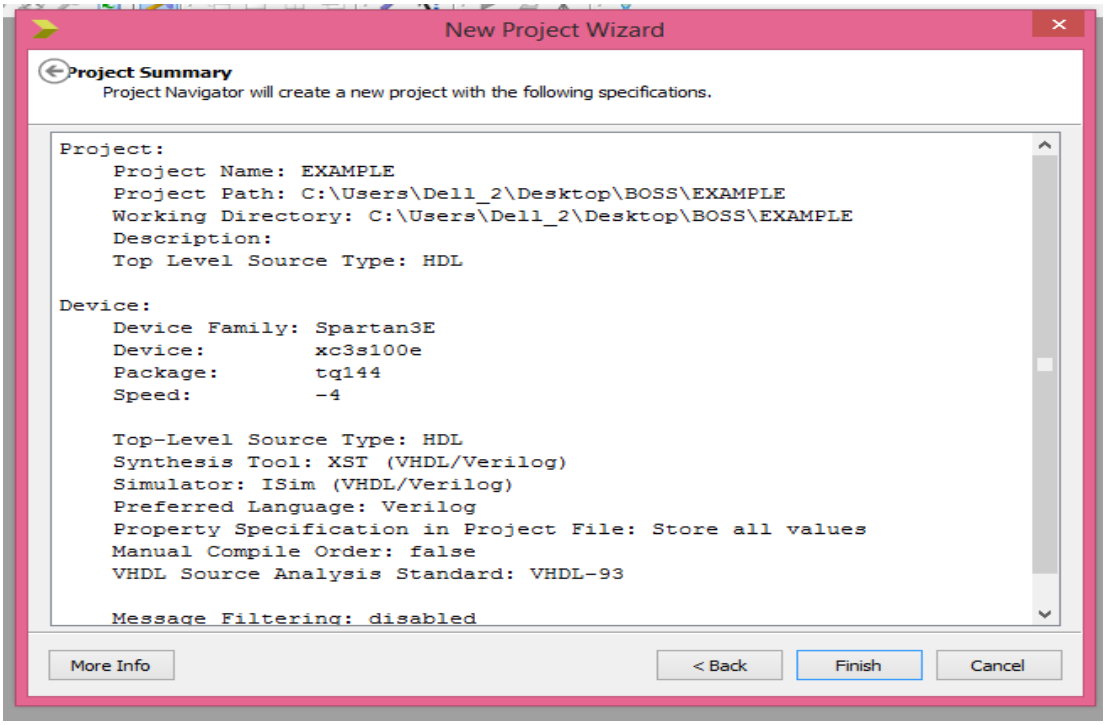




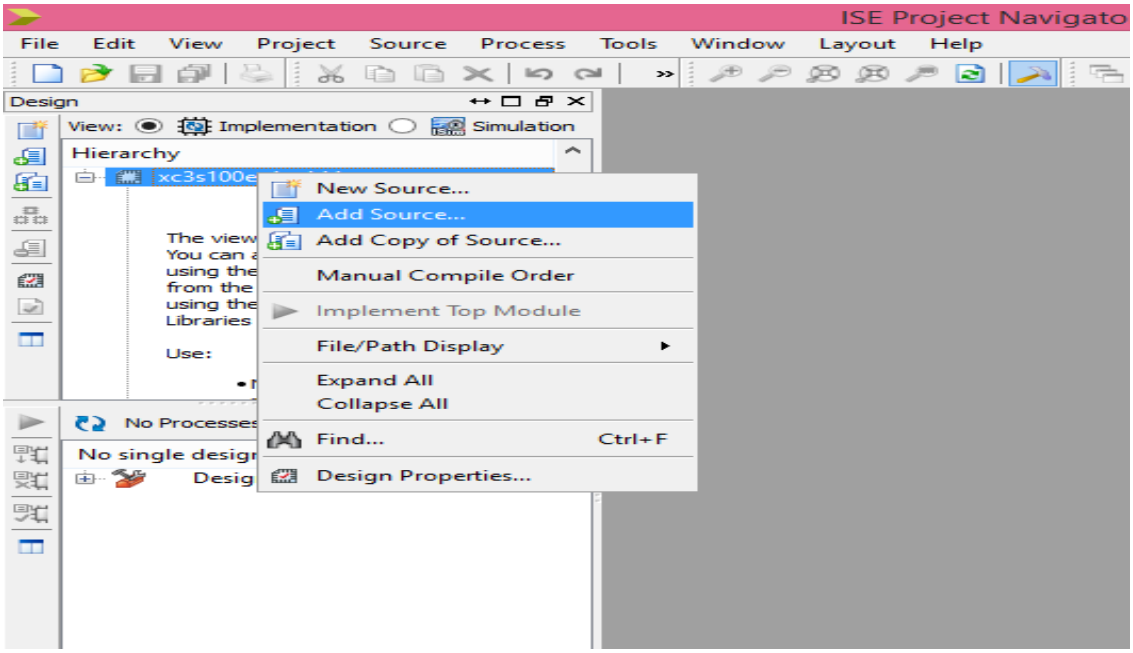
Step 3: CLICK ON NEXT and NEXT



Step 4: CLICK ON FINISH

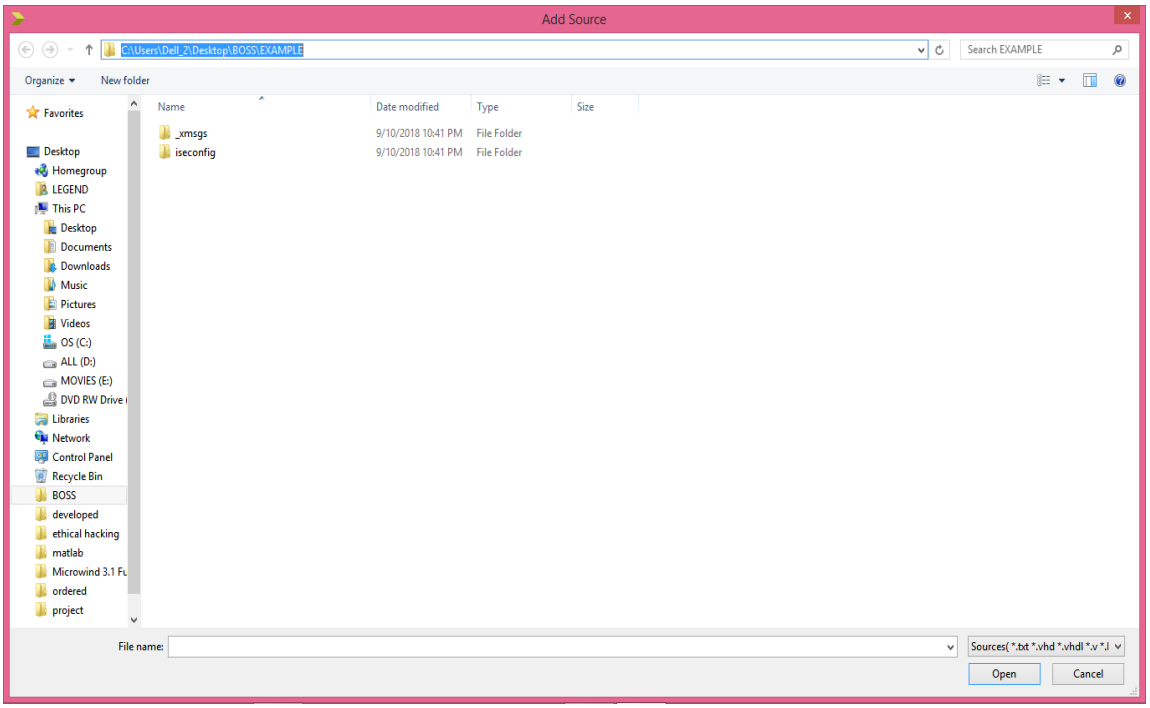


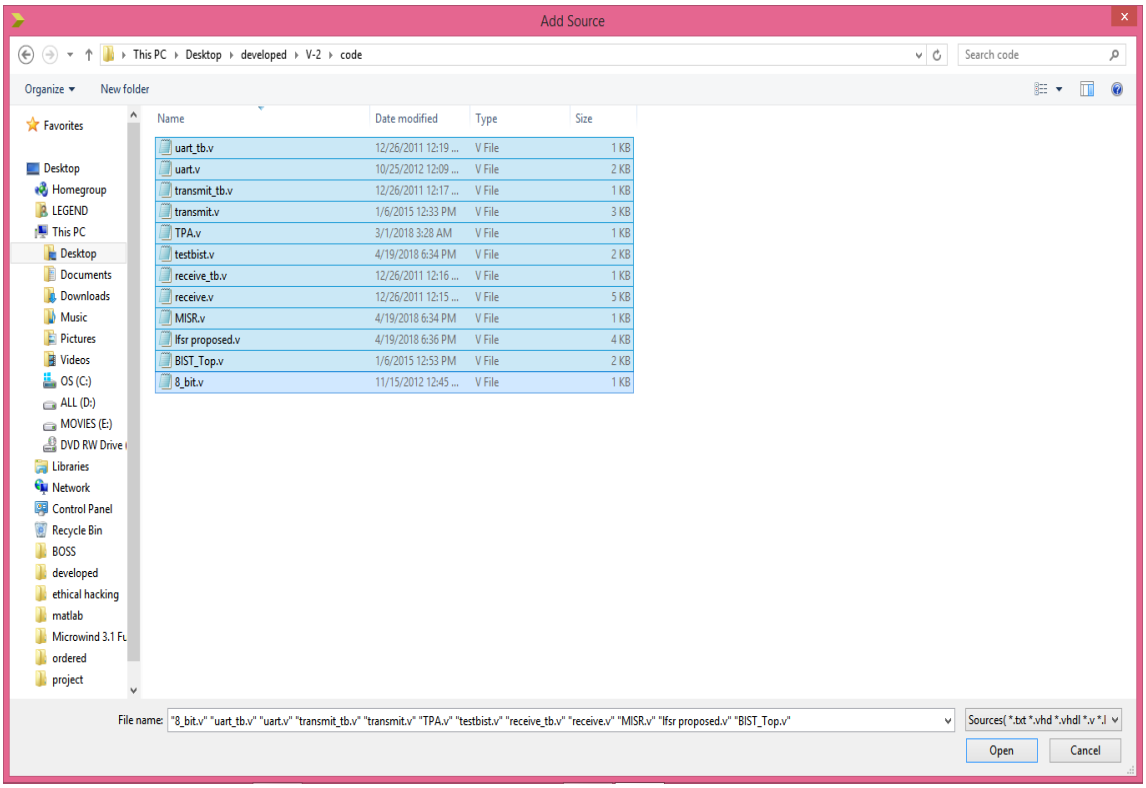
Step 5: CLICK ON CHIP (XC…) then MOUSE RIGHT CLICK then CLICK ON ADD SOURCE



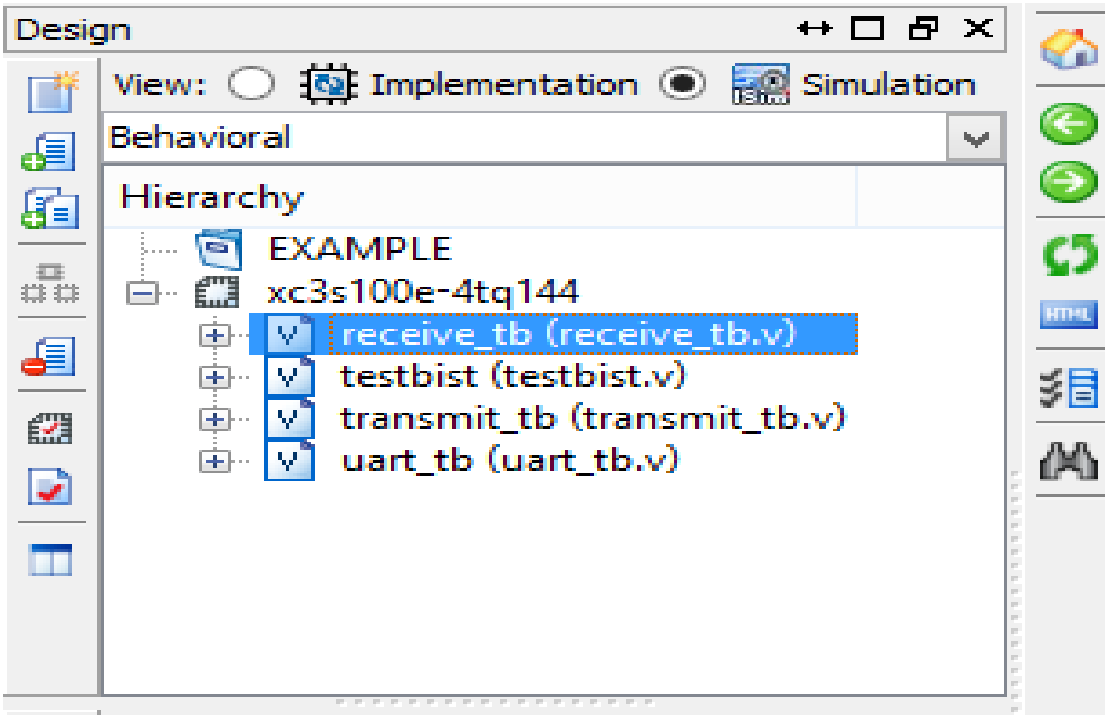
Step 6: SELECT THE CODE LOCATION GIVEN BY DEVELOPER AND ADD CODE

(Note ALL FILES) AND CLICK OPEN



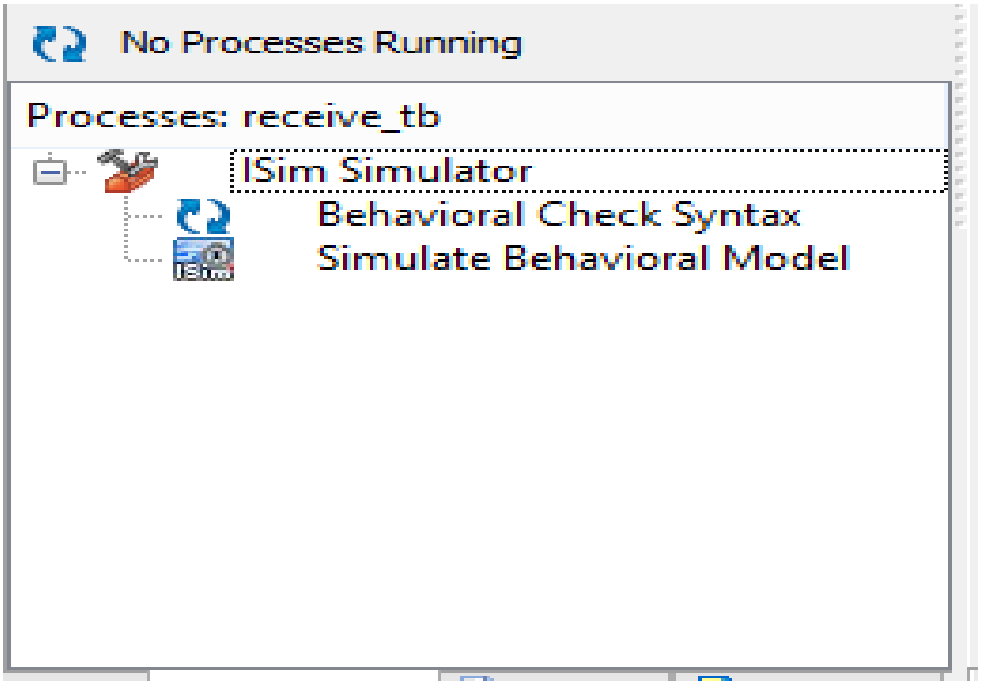


Step 7: SELECT THE SIMULATION and select files to RUN



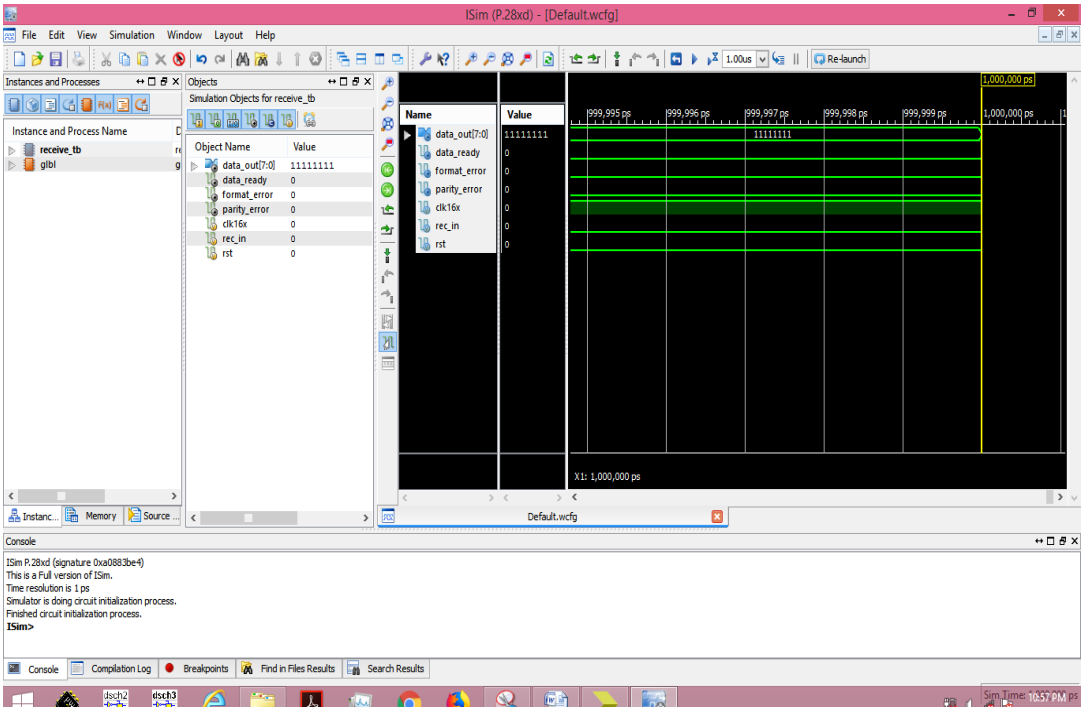
Step 8: SELECT ISIM SIMULATOR and SIMULATE BEHAVIORAL MODEL

If no errors isim window will open



Step 9: ISIM WINDOW

 **select zoom to full view**



CHAPTER 7

RESULTS AND DISCUSSION

Xilinx ISE software was used to create all of the HMF-DC designs. This software programmed gives two types of outputs: simulation and synthesis. The simulation results provide a thorough examination of the HMF-DC architecture in terms of input and output byte level combinations. Decoding procedure approximated simply by applying numerous combinations of inputs and monitoring various outputs through simulated study of encoding correctness. The use of area in relation to the LUT count will be accomplished because of the synthesis findings. In addition, a time summary will be obtained about various path delays, and a power summary will be prepared utilizing the static and dynamic power consumption. Further, MatlabR2020a software is used to evaluate the subjective performance of HMF-DC.

Fig 7.1: - Simulation outcome of HMF-DC.

Figure 7.1 presents the simulation outcome of HMF-DC. Here, P_0, P_1, P_2, P_3, P_4, P_5, P_6, P_7, P_8 are the inputs to HMF-DC and median is the output value.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	437	303600	0%
Number of fully used LUT-FF pairs	0	437	0%
Number of bonded IOBs	81	700	11%

Fig 7.2: - Design summary.

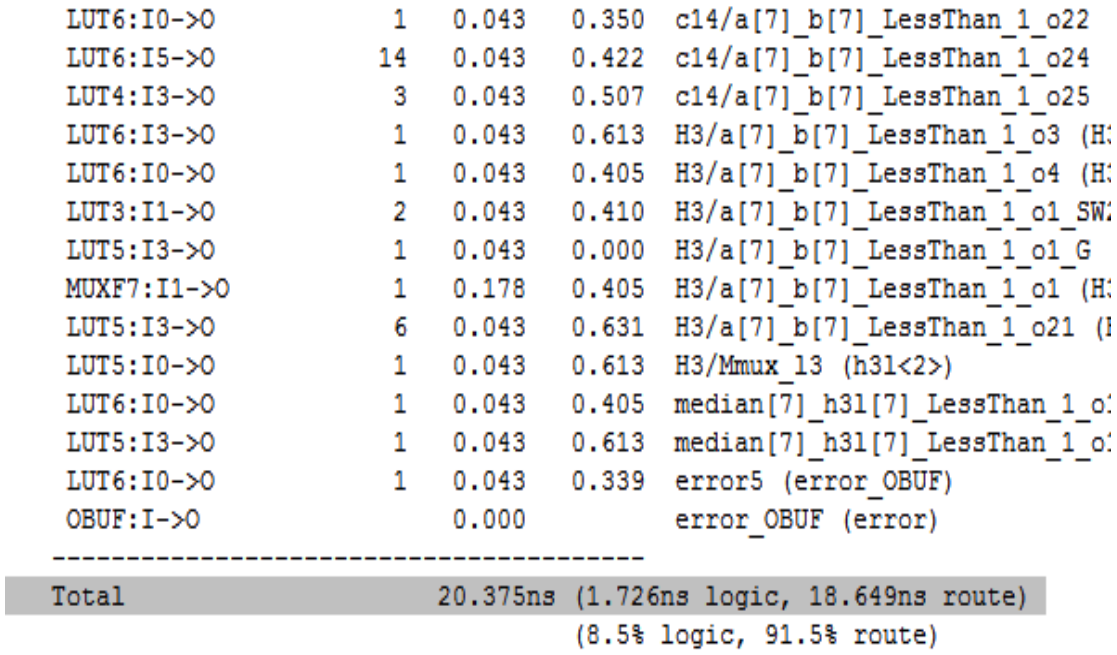


Fig 7.3: - Time summary

Figure 7.2 shows the design (area) summary of proposed method. Here, the proposed method utilizes the low area in terms of slice LUTs i.e., 437 out of available 303600. Figure 7.3 shows the time summary of proposed method. Here, the proposed method consumed total 20.375ns of time delay, where 1.726ns is logical delay, and 18.649ns is route delay. Figure 8 shows the power consumption report of proposed DCM-RTPG-BFD. Here, the proposed DCM-RTPG-BFD consumed power as 32.83 milli watts.

2. Summary

2.1. On-Chip Power Summary

On-Chip Power Summary				
On-Chip	Power (mW)	Used	Available	Utilization (%)
Clocks	1.30	3	---	---
Logic	0.00	10	11776	0
Signals	0.00	20	---	---
IOs	0.00	20	372	5
Quiescent	31.52			
Total	32.83			

Fig 7.4: - Power summary.

Fig 7.5: - Visuval performmace of HMF-DC. (a) original image, (b) noisy image, (c) SMF [18], (d) DMF [21], (e) AMF [25], (d) proposed HMF-DC.

Figure 7.5 shows the filtering performance of various methods like SMF [18], DMF [21], AMF [25], and proposed HMF-DC. Here, SMF [18] and AMF [25] methods resulted outcome still contains the highher noises, DMF [21] method outcome contains the low level noises. But, the proposed HMF-DC method resulted outcome is looks similar to the

original image. Table 7.1 compares the performance evaluation of proposed HMF-DC method. Here, the proposed HMF-DC resulted in superior (reduced) hardware performance in terms of LUTs, time-delay, and power consumption as compared to conventional approaches such as SMF [18], DMF [21], and AMF [25]. Further, the proposed HMF-DC resulted in improved subjective performance in terms of peak signal to noise ratio (PSNR), stctural similarity index metric (SSIM) as compared to conventional approaches such as SMF [18], DMF [21], and AMF [25]. Further, the graphical representation of performance comparison is presented in Figure 7.6.

Metric	**SMF [18]**	**DMF [21]**	**AMF [25]**	**Proposed HMF-DC**
LUTs	767	655	542	437
Time delay (ns)	51.927	43.837	32.735	20.37
Power consumption (mw)	82.61	73.41	58.26	32.83
PSNR (dB)	37.34	42.45	48.38	54.53
SSIM	0.827	0.893	0.927	0.992

Table 7.1 Performance evaluation

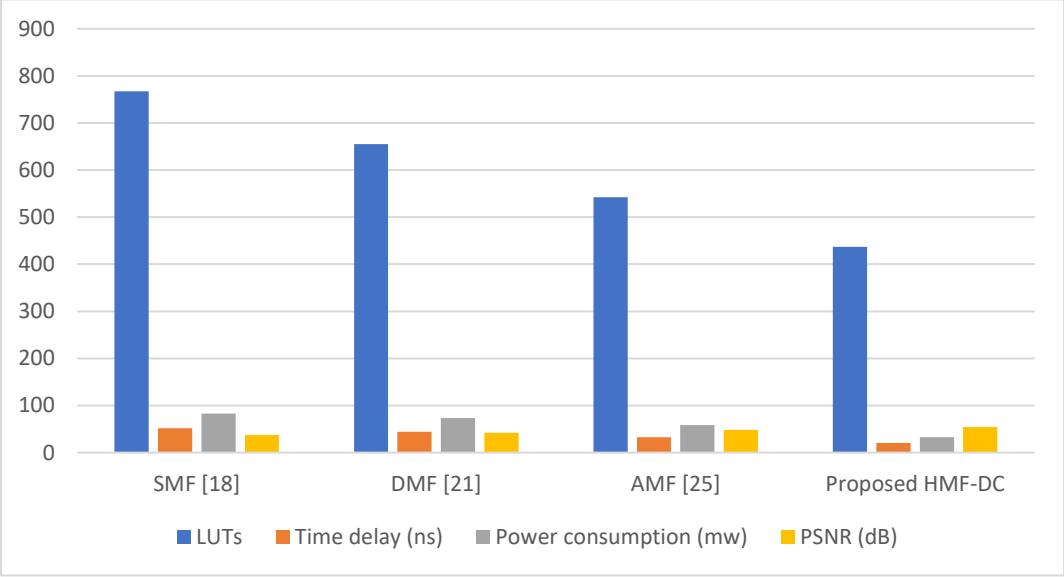


Fig 7.6: - Graphical representation of performance

CHAPTER 8
CONCLUSION AND FUTURE SCOPE

CONCLUSION

The development of a Hybrid Median Filter by making use of Data Comparator logic is the primary emphasis of this study. In the beginning, a multiplexer selection logic-based data comparator is used to determine which of two numbers have high and low values. After then, the data comparator is carried out several times for the nine different possible combinations of pixels, which determines the median value for all nine of those values. The subjective and objective evaluations both reveal that the suggested HMF-DC resulted in greater performance when compared to the state-of-the-art techniques in terms of decreased noise, latency, and power consumption. Hardware metrics such as LUTs were also reduced and software metrics such as PSNR, SSIM are improved using the proposed HMF-DC approach. Further, this work can be extended with the hybrid adaptive filters for improved PSNR performance.

FUTURE SCOPE

This work can be extended with hybrid data sorting methods, which can be consume low area, delay, and power consumptions. Any procedure that includes putting the data into meaningful order to make it simpler to comprehend, analyze, or display the data is referred to as data sorting. When dealing with research data, sorting is a typical strategy used for displaying data in a form that makes it simpler to interpret the narrative being told by the data. This form may be created by putting the data into categories.

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ANNEXTURE

Dear authors,

We received your submission to ICRTAC-2022 (International Conference on Recent Trends in Advanced Computing (ICRTAC-2022)):

Authors: Nikitha and Dr. Divya Gampala
Title : Implementation of hybrid median filtering using hybrid data comparators
Number : 0982

The submission was uploaded by nikithakrishna <nikithakrishna@gmail.com>. You can access it via the ICRTAC-2022 EasyChair Web page

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Thank you for submitting to ICRTAC-2022.

Best regards,
EasyChair for ICRTAC-2022.