Code No: 133AJ

R16

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, May/June - 2019

DIGITAL LOGIC DESIGN

(Common to CSE, IT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) What are 2's complement and 9's complement of a numbers? Give examples. [2]
b) State and prove De Morgan theorems. [3]
c) What are minterms and maxterms? Give examples for each. [2]
d) Define pair quad and octet in K-Maps and give examples. [3]
e) Draw the logic circuit of a full adder and give its truth table. [2]
f) Write the functions of a decoder and multiplexer. [3]
g) Draw the logic diagram of a master slave J-K flip-flop. [2]
h) Describe the race free state assignment in asynchronous sequential circuits. [3]
i) What are PLAs and PALs? [2]
j) Explain about arithmetic operations with examples. [3]

PART-B

(50 Marks)

2.a) Explain various number systems and codes and their conversion with examples for each.
b) Simplify the following Boolean expressions to a minimum number of literals
(i) ABC+A'B+ABC' (ii) xy + x(wz+wz') [5+5]

OR

3.a) Express the following numbers in decimal : $(10110.0101)_2$, $(16.5)_{16}$, $(26.24)_8$.
b) Demonstrate by means of truth tables the Boolean Associative law and distributive law.
c) Simplify the Boolean expression to minimum number of literals: (A+B)' (A'+B'). [10]

4.a) Simplify the following Boolean functions, using a four variable Karnaugh map method and implement the simplified function using NAND gates
$F(A,B,C,D) = \sum 0,2,4,5,6,7,8,10,13,15)$
b) Show that the dual of the exclusive OR is also its compliment. [5+5]

OR

5.a) Draw the multiple level NAND circuit for the following expression:
$(AB'+CD')E + BC(A+B)$
b) Simplify the following four variable Boolean function and implement the same using NAND logic. F (A, B, C, D) = $\sum$ (0, 2, 4, 5, 6, 7, 8, 10, 13, 15) [5+5]

6.a) Construct a 4-bit BCD adder-substractor circuit using BCD adder and 9's complementer.

b) Explain the working and functions of decoders and encoders. Construct 2/4 line decoder with logic gates with enable input. [5+5]

OR

7.a) Construct a 4 bit 2's complement adder using full adders and perform addition and subtraction by taking 4-bit numbers with examples.

b) Explain the design procedure for multiplexers and de-multiplexers and draw the logic diagram of a 4-to-1 line multiplexer with logic gates. [5+5]

8.a) Design 4-bit shift register using D flip-flops and explain its working with the help of timing diagrams.

b) Design a counter with the following repeated binary sequence: 0,1,2,3,4,5,6, use JK flip-flops. [5+5]

OR

9.a) Draw the circuit diagram of a 4-bit binary counter with parallel load and explain its working with its function table.

b) Design a 4 bit synchronous counter with D flip - flops and explain its working. [5+5]

10.a) Given 32 × 8 ROM with enable input, Show the external connections necessary to construct a 128 × 8 ROM with 4 chips and a decoder.

b) Explain the working of a PLA with a schematic and implement the following two Boolean functions with a PLA:
$F_1 (A, B, C) = \sum (0, 1, 2, 4)$ *and* $F_2 (A,B,C) = \sum (0.5.6.7)$. [5+5]

OR

11.a) Explain the functions and applications of PLAs in memory addressing and implement the following two Boolean functions with a PLA:
$F_1 (A, B, C) = \sum (0, 1, 3, 5)$ *and* $F_2 (A, B, C) = \sum (1, 2, 4, 7)$

b) What are sequential programmable devices? Draw the sequential programmable logic for a basic microcell logic. [5+5]

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