R16

Code No: 135AY

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year I Semester Examinations, May/June - 2019

LINEAR AND DIGITAL IC APPLICATIONS

(Common to ECE, EIE)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a)	Define CMRR.	[2]
b)	What are the applications of Schmitt Trigger?	[3]
c)	What is All pass filter?	[2]
d)	Draw the functional block diagram of IC 555 timer.	[3]
e)	Which is the fastest ADC and Why?	[2]
f)	Define Resolution. Give its importance in data converters.	[3]
g)	What is the function of magnitude comparator?	[2]
h)	Define Noise Margin and fan out.	[3]
i)	Write the specifications of counter ICs.	[2]
j)	What are the difference between static and dynamic RAM.	[3]

PART - B

(50 Marks)

2.a) With a neat circuit diagram explain the operation of Schmitt trigger.
b) Draw the internal architecture of IC 723 voltage regulator and explain. [5+5]

OR

3.a) Explain the working of practical and ideal differentiator.
b) Design an op-amp differentiator circuit that varies in frequency from 10Hz to about 1KHz. [5+5]

4.a) With a neat diagram explain about triangular wave generator and derive the frequency of oscillation.
b) Draw the block diagram of PLL and explain in detail. [5+5]

OR

5.a) Explain the operation of monostable 555 timer and derive the expression for the period of pulse generated by the timer.
b) Find the free running frequency if control voltage V_c=10.9V, V_{cc}=12V, R_1=4.6K and C=1.1Nf. [7+3]

6.a) With the help of neat diagram explain the operation of R-2R DAC. Also discuss the disadvantages of Weighted Resistor DAC.

b) Discuss the specifications of ADCs. [5+5]

OR

7.a) With the help of neat diagram explain the operation of Dual slope ADC. What are the disadvantages of parallel comparator type ADC.

b) Calculate the number of bits required to represent a full scale voltage of 10V with a resolution of 5mV approximately. [5+5]

8.a) Draw and explain the working of two input TTL NAND gate and list advantages of totem Pole output stage.

b) Design 16×1 multiplexer using 4×1 multiplexer. [5+5]

OR

9.a) Draw logic level diagram of demultiplexer and then explain the same.

b) Design a Priority encoder circuit and which 74XX series IC is used for it. [5+5]

10.a) Realize D-flip flop using SR flip flop.

b) Design a 3-bit synchronous counter using D-flip flop. [5+5]

OR

11.a) Design and implement FIFO shift register using ICs.

b) Illustrate the architecture of SRAM and then explain the same. [5+5]

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