Code No: 5155C

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech I Semester Examinations, April - 2015
MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN
(Embedded Systems)

Time: 3hrs **Max.Marks:60**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 8 marks and may have a, b, c as sub questions.

PART - A

5 × 4 Marks = 20

1.a) Compare the RISC processor architecture, organization, advantages and drawbacks with respect to CISC processors.
b) List out the branch instructions in ARM processor.
c) What is Thumb instruction set? Explain the various registers usage in ARM Thumb state.
d) Write short notes on basic 'C' Data types in ARM.
e) Draw the diagram of basic ARM memory hierarchy. What is the difference between logical and physical caches?

PART - B

5 × 8 Marks = 40

2. Draw and explain the ARM register set in user mode. Name the special purpose registers and give their function. Draw the format of the CPSR and explain the function of each bit. [8]

OR

3. Give the salient features of ARM7, ARM9, ARM10, and ARM11 family processors. [8]

4. Explain the following ARM instructions with examples.
a) TST b) EOR c) LDMIA d) MSR e) CLZ
f) SWI. [8]

OR

5. Explain the ARM data processing instructions used for arithmetic operations, bit-wise logical operations, register movement operations, and comparison operations with suitable examples. [8]

6. What is ARM thumb instruction set? Explain the use of BX and BLX instructions for switching to thumb state giving an example code. [8]

OR

7. List out the single-register load-store and multiple-register load-store instructions in the thumb instruction set of ARM and explain. [8]

8. Explain the use of FOR loop giving examples for fixed and variable number of iterations. [8]

OR

9. Explain instruction scheduling in ARM using suitable examples. [8]

10. Explain the four-way Set associative cache organization using a neat diagram. [8]

OR

11. Explain the memory organization in a virtual memory system. [8]

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