

R16

Code No: 134AK

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year II Semester Examinations, December - 2019

COMPUTER ORGANIZATION

(Common to CSE, IT)

Time: 3 Hours

Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit.

Each question carries 10 marks and may have a, b as sub questions.

PART - A

(25 Marks)

- 1.a) Define computer. Specify the different types of computers. [2]
- b) Draw the Block diagram of Digital Computer. [3]
- c) How is the addressing mode of an instruction communicated to the CPU? [2]
- d) Write a short note on Machine language instruction formats. [3]
- e) What is the role of stack in calling a subroutine and returning from the routine? [2]
- f) Define a macro SQUARE that calculates the square of a number. [3]
- g) Determine the base of the numbers in each case for the following operations to be correct: $14/2 = 5$. [2]
- h) How the floating-point numbers are represented and used in digital arithmetic operations? [3]
- i) Sometimes processors in tightly coupled multiprocessor environment will be idle. Why? [2]
- j) Differentiate between a conventional scalar processor and a vector processor. [3]

PART - B

(50 Marks)

2. Explain the generic Instruction types present in a computer system. [10]
OR
- 3.a) Compare and Contrast the Computer Design and Computer Architecture. [5+5]
b) Compare hardwired control with microprogrammed control. [10]
4. Elaborate of the Instruction set of 8086. [10]
OR
5. Discuss the physical address formation in different addressing modes. [10]
6. Write an assembly language program to construct a 4 digit decimal number to its binary equivalent, using a procedure for dividing a number by two. [10]
OR
7. Explain interrupt cycle of 8086 and demonstrate interrupt programming. [10]
8. Explain the floating point addition- subtraction unit with a neat diagram. [10]
OR
9. Compare interrupt driven data transfer scheme with DMA. Using block diagram explain interrupt driven transfer scheme. [10]

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- 10.a) Draw a space time diagram for six segment pipeline showing the time it takes to process eight tasks.
- b) Consider the multiplication of two 40×40 matrices using a vector processor.
- i) How many product terms are there in each inner product and how many inner products must be evaluated?
- ii) How many multiply add operations are needed to calculate the product matrix? [5+5]

OR

- 11.a) Explain the parallel processing architecture and its uses.
- b) With the help of a neat diagram explain the match logic for one word of associative memory. [5+5]

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