Code No: 153AG

R18

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, December - 2019
COMPUTER ORGANIZATION AND ARCHITECTURE
(Computer Science and Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a) Differentiate computer organization and architecture. [2]
b) What must the address field of an indexed addressing modes instruction be to make it the same as a registrar indirect mode instruction? [2]
c) Why should the sign of the reminder after a division be the same as the sign of the dividend? [2]
d) How many 128 × 8 RAM chips are needed to provide a memory capacity of 2048 bytes? [2]
e) What are the various physical forms available for establishing an interconnection network? [2]
f) How many references to memory are needed for each type of instruction to bring an operand into a processor register? [3]
g) Is it possible to design a microprocessor without a micro program? Are all micro programmed computers also microprocessors? [3]
h) Represent decimal number 6027 in: i) BCD ii) excess-3. [3]
i) Why are the read and write control lines in a DMA controller bidirectional? Under what condition and for what purpose are they are they used as inputs? [3]
j) Write a short note on array processor. [3]

PART – B

(50 Marks)

2.a) Derive the control gates for the write input of the memory in the basic computer.
b) Design a 4 bit combinational circuit decrementer using four full adder circuits. [5+5]

OR

3. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.
a) How many selection inputs are there in each multiplexer?
b) What sizes of multiplexers are needed?
c) How many multiplexers are there in the bus? [10]

4.a) Make a comparison between the hardwired control and micro programmed control. Is it possible to have a hardwired control associated with a control memory?
b) Explain about Stack Organization in detail. [5+5]

OR

5.a) Draw the block diagram of micro program sequencer for a control memory and explain its operations in detail.

b) How many times does the control unit refer to memory when it fetches and executes an indirect addressing mode instruction if the instruction is:
i) a computational type requiring an operand from memory
ii) a branch type. [5+5]

6.a) Convert the following decimal numbers to binary: 1231; 673; and 1998.

b) Show that there can be no mantissa overflow after a multiplication operation. [5+5]

OR

7. What is floating point representation? Explain the IEEE standard for floating point representation with examples. [10]

8. Explain associative memory hardware organization in detail. [10]

OR

9.a) Give a neat sketch that illustrates the components in a typical memory hierarchy.

b) A computer uses RAM chips of 1024× 1 capacity.
i) How many chips are needed, and should their address lines be connected to provide a memory capacity of 1024 bytes.
ii) How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus. [5+5]

10.a) Discuss the various conflicts that might arise in a pipeline. How are they resolved?

b) Draw and explain the structure of general purpose multicomputer. [5+5]

OR

11. Consider the multiplication of two 40×40 matrices using a vector processor.
a) How many product terms are there in each inner product and how many inner products must be evaluated?
b) How many multiply add operations are needed to calculate the product matrix? [5+5]

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