Code No: 124AF

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year II Semester Examinations, July/August - 2021

DIGITAL DESIGN USING VERILOG HDL

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Answer any Five Questions

All Questions Carry Equal Marks

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1.a) Describe the Role of Verilog as HDL.
b) Explain about the concurrency and data types. [7+8]

2. Differentiate between Simulation and synthesis. Give a brief note on Simulation and synthesis Tools. [15]

3.a) Explain about the continuous assignment structure.
b) Write about the module structure in Gate level modelling. [7+8]

4.a) Explain about the Construction resolution in Gate level modelling.
b) Write about the Array of instance primitives. [7+8]

5.a) Give the behavioural description of a JK Flip flop circuit using an always statement with necessary logic diagram and give Verilog HDL source code.
b) Discuss the following related to behavioural level modelling with necessary syntax and example: (i) Block statement (ii) Case statement. [7+8]

6.a) Give the syntax of 'Always construct' and explain.
b) Write the verilog code for AOI in behavioural model. [7+8]

7.a) Discuss the CMOS switches with examples.
b) With examples, describe file based tasks and functions. [7+8]

8.a) Draw and explain capacitive model of sequential circuit.
b) How to test a combinational circuit? Explain by taking some examples. [8+7]

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