Code No: 5255AP

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech II Semester Examinations, July/August - 2021
DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES
(Embedded Systems)

Time: 3 Hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) Briefly explain the decimation and interpolation process with examples.
b) Explain the sampling process? Also describe why signal sampling is required. [8+7]

2.a) With a neat diagram, explain the DSP computational building blocks
b) Explain the concept of data addressing capability [8+7]

3.a) Explain in detail about Indirect Addressing mode of the TMS320C54XX Processor using Dual memory operands.
b) Briefly explain about program control unit of TMS320C54XX processor. [8+7]

4. Explain pipeline operation of TMS320C54XX processors. [15]

5.a) Explain in detail about the data operations of ARM processor.
b) With a neat diagram, describe the architecture of cortex M4 processor [8+7]

6.a) With a neat diagram, explain the register file of ARM processor.
b) Explain in detail about Nested Vectored Interrupt Controller (NVIC) in detail. [8+7]

7.a) Draw and explain the structural organization of a barrel shifter.
b) With a neat diagram, explain the register file of ARM processor. [8+7]

8.a) With a neat diagram, explain the instruction decode and execution stages in cortex M4 floating point unit.
b) Explain in detail about floating point register bank. [8+7]

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