Code No.: CS403ES | R20 | H.T.No. | | | 8 | R | | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–II–Semester End Examinations (Regular) - June- 2022
ANALOG & DIGITAL ELECTRONICS
(Common to CSE, CSC)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: 1. Answer *any FIVE questions. Each question carries 14 marks.*
2. All questions carry equal marks.
3. Illustrate your answers with NEAT sketches wherever necessary.

5X14=70

1.	a)	Explain Half wave Rectifier with neat diagram.	[8M]
	b)	Explain V-I characteristics of p-n junction diode with effect of temperature.	[6M]
2.	a)	Draw and explain CB amplifier with neat diagram.	[8M]
	b)	Compare Transistor configurations.	[6M]
3.	a)	Explain the operation of Common Drain Amplifier.	[7M]
	b)	Explain the operation of AND, OR, NAND, NOR Gates.	[7M]
4.	a)	Explain the De Morgan theorem.	[6M]
	b)	Draw the logic diagram of 3 to 8 Decoder.	[8M]
5.	a)	Explain the 8X1 MUX.	[8M]
	b)	Simplify the function by using K-Map method for f (A, B, C, D) = $\sum$m (1, 4, 5, 9, 11, 13, 15).	[6M]
6.	a)	Explain the P-N junction diodes.	[8M]
	b)	Draw and explain the Emitter follower with neat diagram.	[6M]
7.	a)	Draw and Explain the V-I characteristics of a JFET.	[8M]
	b)	Explain Binary Multiplier in detail.	[6M]
8.	a)	Explain 3 bit Ripple Counter.	[8M]
	b)	Explain SR latch using NOR gates.	[6M]

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