Code No.: DS305ES | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Supply) - June- 2022
DIGITAL LOGIC DESIGN
(CSD)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: 1. Answer *any FIVE questions. Each question carries 14 marks.*
2. All questions carry equal marks.
3. Illustrate your answers with NEAT sketches wherever necessary..

5X14=70

1	a)	Convert following	
		i. $(111010)_2$ to ($)_{16}$	[2M]
		ii. $(11001)_2$ to EX-3 code.	[2M]
		iii. $(33.125)_{10}$ to binary.	[2M]
		iv. $(111010)_2$ to 2'S complements.	[1M]
	b)	i. What is canonical standard form of Sum of Product (SOP) for f(x, y, z)=x'y'+z and convert into POS form.	[4M]
		ii. Explain and draw the logic symbol of Exclusive-OR and OR gate.	[3M]
2	a)	Simplify function using K-Map method for f (A, B, C, D) = ∑ (0, 1, 3, 5, 7, 8, 9, 11, 13, 15) and draw a logic diagram.	[7M]
	b)	Simplify function using K-Map method for f (A, B, C, D) = ∑ (1, 4, 5, 9, 11, 13, 15) and draw a logic diagram.	[7M]
3	a)	Design full adder.	[7M]
	b)	Design a two-bit Magnitude Comparator.	[7M]
4	a)	i. Compare Latch and Flip-Flop. ii. Compare combinational and sequential circuits.	[7M]
	b)	How many used states and unused state of 4-bit ring counter and draw logic diagram of ring counter.	[7M]
5	a)	Explain the programmable Logic Array.	[7M]
	b)	Explain the random-access memory and discuss with details.	[7M]
6	a)	Design 8X1 MUX.	[7M]
	b)	Design Mod 5 Synchronous counter.	[7M]
7	a)	Simplify function using K-Map method for f (A, B, C) =∑ (0,5,7) +d (1,3) and Draw logic diagram using NAND gates.	[7M]
	b)	Design a Half Adder using OR gates.	[7M]
8	a)	Draw the logic diagram of 3 to 8 Decoder.	[7M]
	b)	Draw a Exclusive-OR gate using NAND gate.	[7M]

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