

Code No.: DS305ES

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H.T.No.

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CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS

II-B.TECH-I-Semester End Examinations (Regular) - January- 2022
DIGITAL LOGIC DESIGN
(CSD)

[Time: 3 Hours]

[Max. Marks: 70]

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 20 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A

(20 Marks)

1. a) Convert Gray to Binary for following [2M]
 - i. 101010,
 - ii. 1100110.
- b) What is Demorgan's Theorem? [2M]
- c) Identify the I, PI, EPI for the given logic $f(A, B, C) = \sum(1, 3, 6, 7)$. [2M]
- d) Draw a Logic Diagram of EXOR Gate using NAND Gates. [2M]
- e) Compare between Combination Circuit and Sequential Circuit. [2M]
- f) How many 4X1 MUX required to implement 32X1 MUX. [2M]
- g) Draw the Truth Table of D Flip Flop. [2M]
- h) How many Used and Unused States for Decade Counter? [2M]
- i) What is PAL? [2M]
- j) What is Memory Decoding? [2M]

PART-B

(50 Marks)

2. Convert following [10M]
 - i. $(10101010)_2$ to Octal,
 - ii. 10100101 to EX-3 Code,
 - iii. $(23.75)_{10}$ to Binary,
 - iv. $(435)_8$ to $()_{16}$,
 - v. $(100001)_{\text{Gray}}$ to Binary.
3. What is Canonical Standard Form of SOP for $f(x,y,z) = xy + x'z$ and convert into POS Form. [10M]
4. Minimize logic function for $f(A, B, C, D) = \sum(1, 3, 4, 6, 9, 11, 12, 14)$ using K-Map. [10M]
5. Minimize logic function for $f(A, B, C, D) = \sum(3, 4, 5, 7, 9, 11, 13, 14, 15)$ using K-Map. [10M]
6. Design a Full Adder using two Half Adders. [10M]
7. Implement Full Adder by using 3X8 Decoder. [10M]
8. What are the disadvantages of S-R Flip Flop, Draw a S-R Flip Flop Logic Diagram and Characteristic Equation. [10M]
9. Design a Mod 5 Synchronous Counter. [10M]
10. What is a Read Only Memory and discuss with detail. [10M]
11. What are advantages of the Programmable Logic Array and discuss with an example. [10M]
