

Code No.: CS8202PC

R20

H.T.No.

8 R

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I-M.TECH-II-Semester End Examinations (Regular) - September- 2022
ADVANCED COMPUTER ARCHITECTURE
(CSE)

[Time: 3 Hours]

[Max. Marks: 70]

- Note:** 1. Answer any FIVE questions. Each question carries 14 marks.
2. All questions carry equal marks.
3. Illustrate your answers with NEAT sketches wherever necessary.

5X14=70

- | | | |
|-------|--|------|
| 1. a) | Explain the Evolution of Computer Architecture. | [7M] |
| b) | List and explain the Program Flow Mechanisms. | [7M] |
| 2. a) | Demonstrate the Evolution of Scalable Computers. | [7M] |
| b) | Assess the Scalability Metrics and Goals. | [7M] |
| 3. a) | Give brief account of Shared Memory Organizations. | [7M] |
| b) | Analyze Superscalar Vs Super pipeline Design. | [7M] |
| 4. a) | Evaluate the Snoopy Bus Protocols. | [7M] |
| b) | Illustrate and Assess the CM-5 Network Architecture. | [7M] |
| 5. a) | Explain the Latency-Hiding Techniques. | [7M] |
| b) | Compare scalable and multithreaded architectures. | [7M] |
| 6. a) | Briefly assess Multi-vector and SIMD Computers. | [7M] |
| b) | Compare and Contrast Hardware vs Software parallelism. | [7M] |
| 7. a) | Outline Scalability of Parallel Algorithms. | [7M] |
| b) | Explain Virtual Memory Technology. | [7M] |
| 8. a) | Explain arithmetic pipeline design. | [7M] |
| b) | Develop Asynchronous and Synchronous Models of Linear Pipeline Processors. | [7M] |
