Code No.: IT301ES | R20 | H.T.No. | | | 8 | R | | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Supply) - August- 2023
ANALOG & DIGITAL ELECTRONICS
(Common to IT, CSM & AI&DS)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a) Explain about PN junction diode. [2M]
   b) What is meant by Half-Adder? [2M]
   c) What is a Thermal Runaway process? [2M]
   d) Define stability. [2M]
   e) What do you understand by universal gates? [2M]
   f) Draw the V-I Characteristics of JFET. [2M]
   g) What are the multiplexers? [2M]
   h) What are the advantages and disadvantages of the K-Map Method? [2M]
   i) What is the difference between Latch And Flip-flop? [2M]
   j) Define clocked sequential circuit. [2M]

PART-B **(50 Marks)**

2. Explain the working principle of tunnel diode with neat sketches? [10M]

OR

3. What are the different types of rectifiers and explain any two rectifiers with waveforms. [10M]

4. With neat sketch explain the voltage divider bias circuit and with operating point. [10M]

OR

5. Explain about RC coupled amplifiers with neat sketch? [10M]

6. Draw the construction of the JFET also with its drain and trans-conductance characteristics? [10M]

OR

7. Compare the TTL, RTL and CMOS Logic families? [10M]

8. Simplify the following expression using the K-map: [10M]
   Y = A'B'C'+ AC'D' + AB'+ ABCD' + A'B'C.

OR

9. Design a 16:1 MUX using 4:1 MUXs. [10M]

10. Design SR Latch and JK flip flop with truth table and logic diagram. [10M]

OR

11. Explain the architecture of Random Access Memory with neat sketch. [10M]

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