Code No.: EC57201PC | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Regular) - September- 2022
ANALOG AND DIGITAL CMOS VLSI DESIGN
(VLSI System Design)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: 1. Answer *any FIVE questions. Each question carries 14 marks.*
2. *All questions carry equal marks.*
3. *Illustrate your answers with NEAT sketches wherever necessary.*

5X14=70

1.	a)	Examine the dynamic behavior of CMOS inverter.	[7M]
	b)	Construct the stick and layout diagram for three input NOR gate.	[7M]
2.	a)	Give a detailed note on floor-planning and placement in the physical design flow of a CMOS circuit design.	[7M]
	b)	Design a 2x1 Mux using CMOS transmission gate logic.	[7M]
3.	a)	Develop a static positive and negative latch based on multiplexers.	[7M]
	b)	Discuss the short channel effects in MOS devices.	[7M]
4.	a)	Analyze the circuit diagram of CS stage with resistive load and derive the voltage gain.	[7M]
	b)	Explain the differential pair with MOS loads.	[7M]
5.	a)	How cascode current mirror circuit is utilized to suppress the channel length effect. Explain?	[7M]
	b)	Explain the source follower circuit and evaluate the input impedance.	[7M]
6.	a)	Draw the basic structure of MOS device and analyze its static behavior.	[7M]
	b)	Discuss the switching threshold and noise margin of static CMOS inverter.	[7M]
7.	a)	Examine the approaches to implement a logic function using ratioed logic.	[7M]
	b)	Summarize the speed and power dissipation in dynamic CMOS logics.	[7M]
8.	a)	Construct the circuit diagram of CMOS master-slave positive edge-triggered register.	[7M]
	b)	Write a short note on the following technologies i. FinFET ii. TFET	[7M]

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