Code No.: EC57201PC | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Regular) - September- 2021
ANALOG AND DIGITAL CMOS VLSI DESIGN
(VLSI System Design)

[Time: 3 Hours] **[Max. Marks: 70]**

1. *Answer Any **FIVE** Questions. Each Question Carries 14 Marks*
2. *All Questions Carry Equal Marks*
3. *Illustrate your answers with NEAT sketches wherever necessary.*

5X14=70

1.	a)	Explain about the quality metrics of digital design.	[7M]
	b)	Write about the wire delay models.	[7M]
2.	a)	Explain about the power analysis in physical design flow.	[7M]
	b)	Describe about the ESD protection mechanism.	[7M]
3.	a)	With necessary diagrams explain about the Bi-stability Priniciple.	[7M]
	b)	Write about the MUX-based latches.	[7M]
4.	a)	Explain about the design of single stage CS amplifier with resistance load.	[7M]
	b)	With a neat diagram Explain about the Gilbert Cell.	[7M]
5.	a)	Give an Brief overview on specifications of active mirror circuits.	[7M]
	b)	Differentiate between active and passive mirror circuits.	[7M]
6.	a)	Explain about the Switching Threshold in MOS Structures.	[7M]
	b)	Explain about the Noise margin concepts in MOS Design.	[7M]
7.	a)	Explain about the Static CMOS design indetail.	[7M]
	b)	Write about the Cascading Dynamic gates.	[7M]
8.	a)	Explain about the concept of pipelining in Sequential logic design.	[7M]
	b)	Write a short note on Metal gate technology.	[7M]

******00******