Code No.: EC57201PC | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Supply) - March- 2023
ANALOG AND DIGITAL CMOS VLSI DESIGN
(VLSISD)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a)	Define noise margin.	[2M]
b)	Recall the wire delay models.	[2M]
c)	Sketch the two input CMOS NAND gate circuit.	[2M]
d)	What is pass transistor logic?	[2M]
e)	Compare FinFet and TFET technologies.	[2M]
f)	Sketch the circuit of static SR Flipflop.	[2M]
g)	Draw the CS stage circuit diagram.	[2M]
h)	How do you operate a source follower as voltage buffer?	[2M]
i)	Why cascade current mirrors are preferred over basic current mirrors?	[2M]
j)	Compare cascade stage and difference pair.	[2M]

PART-B **(50 Marks)**

2.a)	Write a note on quality metrics of digital design.	[5M]
b)	Draw the CMOS inverter circuit and explain in different regions of operation.	[5M]
	OR	
3.	Draw the stick diagram and layout for universal gates.	[10M]
4.	Discuss briefly about CMOS transmission gate and construct multiplexer using transmission gate.	[10M]
	OR	
5.a)	Describe the performance metrics of speed and power consumption of dynamic CMOS logic.	[5M]
b)	With neat sketches, explain the cascading of dynamic gates.	[5M]
6.	Give a short note on the following i) Short channel effects ii) Metal gate technology	[10M]
	OR	
7.	Construct a transistor level Master-Slave edge-triggered register using multiplexers. Explain about the dynamic latches and registers with neat sketches.	[5M] [5M]
8.a)	Analyze the single stage CS amplifier circuit with triode load.	[5M]
b)	Sketch the basic differential amplifier circuit and explain the common mode response.	[5M]
	OR	
9.	Illustrate the small signal equivalent circuit of a degenerated CS stage and derive its voltage gain.	[10M]
10.	Give in detail explanation of active current mirror circuits.	[10M]
	OR	
11.a)	Discuss the Cascade current mirror circuit.	[5M]
b)	Outline the frequency response of CS stage.	[5M]

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