Code No.: CS302PC

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CMR ENGINEERING COLLEGE: : HYDERABAD UGC AUTONOMOUS

II-B.TECH-I-Semester End Examinations (Regular) - February 2023 COMPUTER ORGANIZATION AND ARCHITECTURE (Common to CSE, IT, CSC & CSM)

[Time: 3 Hours]
Note: This question paper contains two parts A and B.

[Max. Marks: 70]

Part A is compulsory which carries 20 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

	PART-A	(20 Marks)
1. a) b) c) d) e) f) g) h) i)	Write some of the components of a Microprocessor. What is Computer Architecture? Write any two Micro program examples. Explain the Instruction Format. Find the 2's complement of 10010. What are the Decimal Arithmetic Operations? Explain DRAM. What is the Input-Output Interface? Define Inter-Processor Arbitration. Write any two characteristics of RISC.	[2M] [2M] [2M] [2M] [2M] [2M] [2M] [2M]
•	PART-B	(50 Marks)
2. a) b)	Explain Arithmetic Logic Shift unit with an example.	[5 M]
U)	What is an Interrupt? Explain about various types of Interrupts.	[5 M]
3.a)	What is Shift Register? Explain the general capabilities of Shift Registers.	[5M]
b)	Discuss about Memory Reference Instructions.	[5M]
4.	Explain the basic organization of a Micro-programmed Control Unit and the generation of Control Signals using Micro-program.	[10M]
5.	OR Describe the Control Unit Organization with a separate Encoder and Decoder functions in a	5100.43
	hardwired control.	[10M]
6.	Explain Booth Multiplication Algorithm with an example.	[10M]
-	OR	[10141]
7.	Discuss Arithmetic addition and subtraction with signed-2's complement representation.	[10M]
8.a)	Discuss Direct Memory Access (DMA).	[5M]
b)	Explain Interrupt Initiated Input-Output.	[5M]
9.	OR List any six ways of improving the Cache Memory performance.	510343
	2.55 may 5 of improving the cache Memory performance.	[10M]
10.	Explain the differences between CISC and RISC.	[10M]
11.	OR	
11.	What are Multiprocessors? Mention the categories of Multiprocessors? Explain Single Instruction Stream and Multiple Data Stream (SIMD).	[10M]