Code No.: DS405PC

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CMR ENGINEERING COLLEGE: : HYDERABAD UGC AUTONOMOUS

II-B.TECH-II-Semester End Examinations (Regular) - August- 2023 COMPUTER ORGANIZATION AND ARCHITECTURE (CSD)

[Time: 3 Hours] [Max. Marks: 70]

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 20 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

	PART-A	(20 Marks)
1. a) b) c) d) e) f)	List out the four main functions of a computer. What are the basic components of register transfer logic? Define address sequencing? Distinguish between auto increment and auto decrement addressing mode. State the condition for floating-point number to become normalized. Perform the following operation on signed numbers using 2's compliment meth (56) ₁₀ +(-27) ₁₀ . State the drawbacks of programmed I/O and interrupt driven I/O. Explain memory hierarchy? What would be the effect, if we increase the number of pipelining stages?	[2M] [2M] [2M] [2M] [2M] od: [2M] [2M] [2M] [2M] [2M]
j)	Define the cache incoherence.	
2.	PART-B Draw the functional diagram of a computer and explain each block.	(50 Marks) [10M]
3.a) b)	OR What is Register Transfer? Explain the read memory and write memory operations. What is a logic micro operation? Discuss in detail various types of logic micro operatio	[5M] ns. [5M]
4.a) b)	List and explain the functions of control unit. Illustrate the use of various addressing modes with examples. OR	[5M] [5M]
5.a) b)	Describe the general register organization. Discuss the two techniques to design the control unit	[5M] [5M]
6.	Explain in detail about floating point representation. OR	[10M]
7.	Explain about Booth's multiplication algorithm and solve Multiply 7 and 3.	[10M]
8.	Explain the I/O instructions and type of I/O instructions. OR	[10M]
9.a) b)	Explain the Direct mapping techniques in cache memory with an example. Explain about Direct Memory Access (DMA).	[5M] [5M]
10.	Give the major characteristics of RISC and CISC architectures. OR	[10M]
11.a) b)		[5M] [5M]