Code No.: R22EC~~57204PE43~~ 57243PE

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CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Regular) – September- 2023
DESIGN FOR TESTABILITY
(VLSI SD)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1. a) Define Testing. [1M]
   b) Define Defect. [1M]
   c) What is meant by simulation? [1M]
   d) What is ATPG? [1M]
   e) What is Digital DFT? [1M]
   f) What is Partial scan design? [1M]
   g) Define Test per clock. [1M]
   h) Draw the block diagram for a BIST. [1M]
   i) Define Boundary scan. [1M]
   j) What is BDSL? [1M]

PART-B **(50 Marks**

2. Explain the different types of testing. [10M]

OR

3. Define the following fault models using examples. [10M]
   i) Cross – Pint Fault ii) Multiple stuck – at fault iii) Transition fault.

4. Explain the problems in simulation –based design verification. [10M]

OR

5. Explain what action an event-driven true-value simulator will take when it evaluates a zero-delay gate. [10M]

6. How the control logic can be used to increase the observability and controllability? [10M]

OR

7. Explain about Ad-Hoc design for testability techniques. [10M]

8. How mutual comparator is useful in memory BIST when the memory system has multiple arrays? [10M]

OR

9. Draw the block diagram for a BIST implementation using BILBO and explain the test procedure. [10M]

10. Explain the Boundary Scan standards. [10M]

OR

11. Explain about TAP controller used in test-bus circuitry. [10M]

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