Code No.: EC57204PE | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Regular) - September- 2022
DESIGN FOR TESTABILITY
(VLSI System Design)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: 1. Answer *any FIVE questions. Each question carries 14 marks.*
2. All questions carry equal marks.
3. Illustrate your answers with NEAT sketches wherever necessary.

5X14=70

1.	a)	Discuss in detail about levels of fault models.	[7M]
	b)	Explain the role of testing in VLSI System design.	[7M]
2.	a)	Illustrate different algorithms for True-Value simulation.	[7M]
	b)	Write a short note on ATPG.	[7M]
3.	a)	Differentiate Scan Design and Partial-Scan Design.	[7M]
	b)	Explain the variations of scan in detail.	[7M]
4.	a)	Discuss about the steps involved in BIST process.	[7M]
	b)	Write a short note on Circular Self Test Path System.	[7M]
5.	a)	Explain the need of Boundary Scan Standard.	[7M]
	b)	Discuss about boundary scan test instructions.	[7M]
6.	a)	Discuss how VLSI technology trends affecting testing.	[7M]
	b)	Compare different types of Testing in VLSI system Design.	[7M]
7.	a)	Illustrate different algorithms for fault simulation.	[7M]
	b)	Write a short note on Test evaluation.	[7M]
8.	a)	What are the high level testability measures?	[7M]
	b)	Explain Ad-Hoc DFT methods in detail.	[7M]