Code No.: EC57204PE | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Regular) - September- 2021
DESIGN FOR TESTABILITY
(VLSI System Design)

[Time: 3 Hours] **[Max. Marks: 70]**

1. *Answer Any **FIVE** Questions. Each Question Carries 14 Marks*
2. *All Questions Carry Equal Marks*
3. *Illustrate your answers with NEAT sketches wherever necessary.*

5X14=70

1.	a)	Explain Digital and Analog VLSI Testing?	[7M]
	b)	Write and Explain the types of Testing?	[7M]
2.	a)	What is Algorithm for True-Value Simulation?	[7M]
	b)	Explain Simulation Design Verification and Test Evaluation?	[7M]
3.	a)	What is DFT? Why it is required?	[7M]
	b)	Explain SCOAP Controllability and Observability?	[7M]
4.	a)	Explain Test –Per – Scan BIST Systems?	[7M]
	b)	What is Pattern Generation?	[7M]
5.	a)	Explain System Configuration with Boundary Scan?	[7M]
	b)	Discuss the BDSL Description Components?	[7M]
6.	a)	Illustrate economic case for BIST?	[7M]
	b)	Explain about ring Configuration of TAP Controller?	[7M]
7.	a)	Explain in detail about Temporary Faults?	[7M]
	b)	Inspect the Ad-Hoc DFT methods?	[7M]
8.	a)	Explain Digital DFT and Scan Design?	[7M]
	b)	What are the Boundary Scan Test Instructions?	[7M]

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