Code No.: EC57101PC | R22 | H.T.No. | | | 8 | R | | | | | |

# CMR ENGINEERING COLLEGE: : HYDERABAD
## UGC AUTONOMOUS
## I–M.TECH–I–Semester End Examinations (Regular) - March- 2023
## DIGITAL DESIGN & VERIFICATION
## (VLSISD)

**[Time: 3 Hours]** **[Max. Marks: 60]**

**Note:** This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

**PART-A** **(10 Marks)**

1. a) Define Encoder? [1M]
   b) Define Multiplexer? [1M]
   c) Give the main difference between Verilog HDL and VHDL. [1M]
   d) Write the Test Bench to AND Gate Program. [1M]
   e) How can you implement Case Studies in System Verilog. [1M]
   f) What is meant by Tickle File (Tcl). [1M]
   g) Define IR drop. [1M]
   h) What is meant by Electromigration? [1M]
   i) What is FPGA? [1M]
   j) What are the advantages of PLA over ROM. [1M]

**PART-B** **(50 Marks)**

2. Explain the two types of Synchronous State Machines. [10M]

**OR**

3. What is meant by Metastability? Explain how to avoid Metastability in Digital Circuits. [10M]

4. Discuss about Non Blocking Assignments with suitable examples of Verilog HDL. [10M]

**OR**

5. Define Logic Synthesis? Draw the Flow Chart of Logic Synthesis. What is the impact of Logic Synthesis? [10M]

6. Explain how the Test Bench is connecting to the Design with example. [10M]

**OR**

7. What is the difference between System Verilog and Verilog HDL?How to initialize a Static Variable in a Task in System Verilog? Explain. [10M]

8. Discuss about various types of Roots of Challenges in Physical Design. [10M]

**OR**

9. a) Explain about Crosstalk Noise and Crosstalk Delay. [5M]
   b) Discuss about Coarse Grained Reconfigurable Devices. [5M]

10. Distinguish between PAL and PLA. [10M]

**OR**

11. Give a brief note on Antifuse and SRAM. [10M]

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