Code No.: EC57101PC | R20 | H.T.No. | | | 8 | R | | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–I–Semester End Examinations (Supply) - September- 2021
DIGITAL DESIGN AND VERIFICATION
(VLSI System Design)

[Time: 3 Hours] **[Max. Marks: 70]**

1. *Answer Any **FIVE** Questions. Each Question Carries 14 Marks*
2. *All Questions Carry Equal Marks*
3. *Illustrate your answers with NEAT sketches wherever necessary.*

5X14=70

1. a. Illustrate the two modes of asynchronous sequential machines
   b. Write a short note on Booth's Multiplier and Barrel Shifter

2. a. Differentiate between VHDL and System Verilog with example.
   b. Explain about the salient features of the analog language and Mixed-signal language

3. a. Explain with suitable example the procedural statements.
   b. Write verilog code for modeling 3 bit counter. Also write the testbench for testing the design

4. a. Explain different steps in physical design flow.
   b. Describe Signal Integrity analysis and Issues in digital systems.

5. a. Differentiate PLA & PAL devices along with their architecture
   b. Explain about the FPGA Programmable Interconnection Topologies.

6. a. Write verilog code for modeling 4:1 multiplexer. Also write the testbench for testing the design
   b. Explain EPROM based FPGA structure in brief

7. a. While randomizing the stimulus to a design which factors are to be considered? Explain
   b. Explain in detail how to use static variable in System Verilog.

8. a. Explain in brief different challenges of a physical design flow
   b. Write a short note on Electromigration Analysis in VLSI.