Code No.: EC57101PC | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–I–Semester End Examinations (Regular) - April- 2022
DIGITAL DESIGN & VERIFICATION
(VLSI SD)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a)	Write differences between Task and Function.	[2M]
b)	Illustrate Array of Instances of Primitives with an example.	[2M]
c)	What are Tristate Gates?	[2M]
d)	Mention Data Types used in Verilog HDL.	[2M]
e)	Write any two Sequential Models can be used.	[2M]
f)	Write about Bidirectional Gates.	[2M]
g)	What are Parallel Blocks?	[2M]
h)	What are Time Delays with Switch Primitives?	[2M]
i)	Draw the diagram of NAND Gate using CMOS Switches.	[2M]
j)	Write Verilog code using Case Statement.	[2M]

PART-B **(50 Marks)**

2.	Illustrate the two Modes of Asynchronous Sequential Machines.	[10M]
	OR	
3.	Differentiate between VHDL and System Verilog with example.	[10M]
4.	Explain the Procedural Statements with suitable example.	[10M]
	OR	
5.	Write Verilog code for Modeling 3 Bit Up Counter. Also write the Test bench for testing the design.	[10M]
6.	Explain different steps in Physical Design Flow.	[10M]
	OR	
7.	Explain Booth's Multiplier with diagram.	[10M]
8.	Differentiate PLA & PAL devices along with their architecture.	[10M]
	OR	
9.	Explain about the FPGA Programmable Interconnection Topologies.	[10M]
10.	Write Verilog code for Modeling 4:1 Multiplexer. Also write the Test bench for testing the design.	[10M]
	OR	
11.	Explain different challenges of a Physical Design Flow in brief.	[10M]

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