Code No.: DS305ES | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Regular) - February- 2023
DIGITAL LOGIC DESIGN
(CSD)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a)	Convert the $(AE)_{16}$ hexadecimal number to decimal.	[2M]
b)	Simply the Boolean function to minimum number of literals f(a,b,c)=ab'+bc'+a'c.	[2M]
c)	Reduce the Boolean expression f(x,y,z)=$\sum$m(0, 2, 3, 5) using K-map.	[2M]
d)	Draw the logic diagram of EX-OR using NAND gate.	[2M]
e)	Design 4X1 MUX.	[2M]
f)	List out the Application of Encoder.	[2M]
g)	What is race around condition?	[2M]
h)	Compare synchronous and asynchronous counters.	[2M]
i)	Write about random-access memory.	[2M]
j)	Write about programmable array logic.	[2M]

PART-B **(50 Marks)**

2. i. Convert the $(546)_8$ octal number to decimal and also binary number. [10M]
   ii. Subtract $(6E)_{16}$ from $(C5)_{16}$ using twos complements method.

OR

3. Convert SOP to POS for F(X,Y,Z)=XY'+ZY'+X'+X. [10M]

4. Reduce the following function [10M]
   i. F(A, B, C, D)=$\sum$m(2, 4, 6, 8, 9, 11,13,15) using K Map.
   ii. F(A ,B, C, D)=$\sum$m(1,5,9,11,13)+d(3,6,8) using K Map.

OR

5. Reduce the Boolean expression using K-map and implement expression in NAND gate F(A,B,C,D)=πM(1, 2, 3, 4, 5, 9, 11)+d(2, 4, 8). [10M]

6. Design Half adder and implement using NOR Gates. [10M]

OR

7. Design 2 bit Magnitude comparator. [10M]

8. Explain the JK flip flop with characteristic table and excitation table. [10M]

OR

9. Design 3 bit synchronous up counter using negative edge trigger. [10M]

OR

10. Explain about memory decoding in detail. [10M]

OR

11. Explain about Programmable Logic Array in detail. [10M]

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