Code No.: EC302PC | R20 | H.T.No. | | | 8 | R | | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Regular) - February- 2023
DIGITAL SYSTEM DESIGN
(ECE)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a)	Convert the binary number 101101 in to Gray code.	[2M]
b)	Explain about Canonical SOP and POS forms.	[2M]
c)	What is K-Map? How it is used to simplify Boolean expressions?	[2M]
d)	Design 2 bit magnitude comparator.	[2M]
e)	What are the important applications of counters?	[2M]
f)	Draw the PIPO shift register.	[2M]
g)	Realize $F(x,y,z) = \Sigma m(1,2,5,7)$ using PLA.	[2M]
h)	Find the number of address lines to access 4KB ROM.	[2M]
i)	Draw the DTL OR gate.	[2M]
j)	Define noise margin.	[2M]

PART-B **(50 Marks)**

2.	Why modern computers use 2's complement scheme for subtractions? Explain in detail by giving suitable examples.	[10M]
	OR	
3.	For the given logic equation, implement with three NOR –gates Y=(A+B) . (C+D).	[10M]
4.	Simplify the Boolean function using k-map in SOP and POS forms $F=\sum m(0,1,2,4,7,8,12,14,15,16,17,18,20,24,28,30,31)$.	[10M]
	OR	
5.	Implementing a 4-input function with a multiplexer $F(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$.	[10M]
6.	Define the following terms with relation to flip flop (i) Setup time (ii) Hold time (iii) Propagation delay time (iv) Preset state (v) Clear state.	[10M]
	OR	
7.	Draw the functional diagram of a 3 bit synchronous up down counter using JK flip flops.	[10M]
8.	Design binary sequence detector which recognizes four consecutive 1's. Draw the state diagram, state table and design a circuit.	[10M]
	OR	
9.	Design BCD to XS3 code converter using a (i) PROM (ii) PLA and (iii) PAL.	[10M]
10.	What is meant by Tristate logic? Draw the circuit of Tristate TTL logic and explain the functions.	[10M]
	OR	
11.	Implement NOT, NAND and NOR logic operation using CMOS logic family.	[10M]

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