Code No.: EC302PC

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CMR ENGINEERING COLLEGE: : HYDERABAD UGC AUTONOMOUS

II-B.TECH-I-Semester End Examinations (Supply) - August- 2023 DIGITAL SYSTEM DESIGN

(ECE)

[Time: 3 Hours] [Max. Marks: 70]

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 20 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

	PART-A	(20 Marks)
1. a) b)	Convert the Gray coded number 1011010111001 in to Binary. How can you get the Boolean equations from the truth table?	[2M] [2M]
c)	Describe the importance of don't care conditions.	[2M]
ď)	What is the draw back in binary parallel adder? How can it be rectified?	[2M]
e)	What is meant by Race Around condition in flip flop?	[2M]
f)	Mention some important applications of shift registers.	[2M]
g)	What is a PLA? Describe its uses.	[2M]
h)	Describe the basic functions of ROM.	[2M]
i)	Draw the symbol of NMOS and PMOS transistor.	[2M]
j)	Define Propagation delay.	[2M]
	PART-B	(50 Marks)
2.	How hamming codes locate the error? Explain with an example.	[10M]
	OR	5403.57
3.	What is Boolean algebra? How it is different from ordinary algebra and bin number system.	ary [10M]
4.	Minimize the following function using K-Map.	[10M]
	$F(w,x,y,z) = \sum m(0,1,2,3,4,6,8,9,10)$ OR	
5.		[10M]
٥.	Design 4-bit BCD to XS-3 code converter.	[10M]
6.	Explain the operation of JK Master slave flip flop. OR	[10M]
7.	What is a shift register? Explain different types of shift registers with function	onal [10M]
	diagrams.	
8.	Derive the state table and state diagram for a serial adder. OR	[10M]
9.	Compare three combinational circuits PLA, PAL and ROM.	[10M]
10.	Compare different CMOS Logic families.	[10M]
	OR	_
11.	Explain the following specifications	[10M]
	i. Fan out ii. Noise margin.	
