UGC AUTONOMOUS

III–B.TECH–II–Semester End Examinations (Regular) - May- 2023

FPGA PROGRAMMING

(ECE)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a)	Summarize FPGA routing using SRAM bits.	[2M]
b)	Outline architectural difference between PLA and PAL.	[2M]
c)	Conclude the need of System Integration and Test.	[2M]
d)	Explain importance of Simulation and synthesis in the design flow to reach UDM design goals.	[2M]
e)	Contrast the significance of *next* and *exit* constructs in VHDL.	[2M]
f)	Distinguish between casex and casez constructs in Verilog.	[2M]
g)	Identify various Bidirectional Switches supported in verilog.	[2M]
h)	How to declare global constants Generic in VHDL and Parameter in Verilog.	[2M]
i)	Justify "synthesizable design should consist only functions but not task".	[2M]
j)	Define setup time.	[2M]

PART-B **(50 Marks)**

2.	Explain the function block in a CPLD.	[10M]
	OR	
3.	Demonstrate Configurable I/O Blocks in FPGA.	[10M]
4.	Illustrate the Design Flow of UDM-PD.	[10M]
	OR	
5.	Explain the Role of verification in UDM-PD and the various steps in verification.	[10M]
6.a)	Construct VHDL Code for Behavioral Description of a D-Latch Using Signal-Assignment Statements and if statement.	[5M]
b)	Construct Data flow HDL Code of a 2x4 Decoder.	[5M
	OR	
7.	Develop data flow HDL verilog Code for a 2x2 Unsigned Combinational Array Multiplier.	[10M]
8.a)	Model Switch-level description of a 2x1 Multiplexer with active high enable.	[5M]
b)	Model a Structural description of a full adder.	[5M]
	OR	
9.a)	Construct Structural description of a three-bit ripple-carry adder.	[5M]
b)	Construct switch level HDL Code for a Two-Input NAND Gate using VHDL.	[5M]
10.a)	Contrast the features of tasks and functions supported in verilog.	[6M]
b)	Write short notes on formal verification.	[4M]
	OR	
11.	Build HDL behavioral description of a full adder using procedure and task.	[10M]

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