Code No.: EC57202PC | R20 | H.T.No. | | | 8 | R | | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Regular) – September - 2021
LOW POWER SYSTEM DESIGN
(VLSI System Design)

[Time: 3 Hours] **[Max. Marks: 70]**

1. *Answer Any **FIVE** Questions. Each Question Carries 14 Marks*
2. *All Questions Carry Equal Marks*
3. *Illustrate your answers with NEAT sketches wherever necessary.*

5X14=70

1.	a)	Analyze the sources of leakage power with neat diagram.	[7M]
	b)	Explain how threshold voltage is adjusted for the CMOS structures.	[7M]
2.	a)	Explain power consumption in flip flops?	[7M]
	b)	Explain the power dissipation in clock distribution?	[7M]
3.	a)	Show the differences between carry select adders and carry save adders.	[7M]
	b)	Discuss any two types of low voltage low power logic styles.	[7M]
4.	a)	Discuss sources and reduction of power dissipation in memory subsystems	[7M]
	b)	Discuss low power SRAM technologies with neat diagrams.	[7M]
5.	a)	Explain implementation problem for low power microprocessor design system	[7M]
	b)	Discuss power management support and architectural trade offs for power in microprocessor design system	[7M]
6.	a)	What is the impact of technology scaling .Write the advantages of Voltage scaling.	[7M]
	b)	Define the effects of Vdd and Vt on speed of CMOS circuits?	[7M]
7.	a)	Explain reversible pipelines in low power circuit techniques?	[7M]
	b)	Write about high capacitance nodes in Low power VLSI circuits?	[7M]
8.	a)	Draw the basic building blocks of the Baugh-Wooley multiplier architecture and explain its operation?	[7M]
	b)	Explain power minimization techniques?	[7M]