Code No.: EC57202PC | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Regular) - September- 2022
LOW POWER SYSTEM DESIGN
(VLSI System Design)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: 1. Answer *any FIVE questions. Each question carries 14 marks.*
2. All questions carry equal marks.
3. Illustrate your answers with NEAT sketches wherever necessary.

5X14=70

1.	a)	Analyze the effects of V_{DD} and V_T on speed.	[8M]
	b)	Describe the impact of technology scaling.	[6M]
2.	a)	Describe the Power consumption in flip-flops and latches.	[7M]
	b)	Describe the power dissipation in clock distribution.	[7M]
3.	a)	Analyze the logic synthesis for low power estimation techniques.	[7M]
	b)	Discuss Low power arithmetic components of multipliers.	[7M]
4.	a)	Explain the concept of Low-Power Memory design?	[7M]
	b)	Discuss the sources of power dissipation in SRAM.	[7M]
5.	a)	Compare different microprocessors in terms of power and performance.	[6M]
	b)	Explain the concepts of low power microprocessor design.	[8M]
6.	a)	Describe the sources of power dissipation in digital IC's.	[7M]
	b)	Discuss recurring themes in low power circuits.	[7M]
7.	a)	Explain the different approaches of Low power design at circuit level.	[7M]
	b)	Discuss the types of energy recovery in CMOS circuits.	[7M]
8.	a)	Explain the Low power arithmetic components circuit design styles.	[7M]
	b)	Discuss briefly about power minimization techniques in low power design.	[7M]

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