Code No.: EC57102PC | R22 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–I–Semester End Examinations (Regular) - March- 2023
MICROCONTROLLERS & PROGRAMMABLE DIGITAL SIGNAL PROCESSORS
(VLSISD)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1.	a)	Identify the role of Link Register in ARM Cortex-M3?	[1M]
	b)	List the Bit-Band Memory regions supported by ARM Cortex-M3.	[1M]
	c)	Recall the highest priority exception of ARM Cortex-M3.	[1M]
	d)	Interpret any one method used by ARM Cortex-M3 to improve the interrupt Latency.	[1M]
	e)	What is the purpose of the LPC 17xx family of microcontrollers?	[1M]
	f)	List the applications of GPIO module in LPC 17xx family of microcontrollers.	[1M]
	g)	How does the barrel shifter function in a programmable DSP?	[1M]
	h)	Give some examples of how programmable DSP can be used.	[1M]
	i)	Describe the benefits of VLIW architecture.	[1M]
	j)	How does pipelining progress through its various phases?	[1M]

PART-B **(50 Marks)**

2.		Explain the following 16-bit instructions of ARM Cortex-M3 i. BIC ii. MVN iii. ROR iv. STRH v. WFI	[10M]
		OR	
3.	a)	Illustrate the Bit-Band operations of ARM Cortex-M3 and mention its advantage.	[5M]
	b)	Examine the three-stage pipeline of ARM Cortex-M3.	[5M]
4.	a)	Categorize and explain the fault exceptions of ARM Cortex-M3.	[5M]
	b)	Describe the need of SYSTICK Timer in ARM Cortex-M3.	[5M]
		OR	
5.	a)	Identify the Interrupt/Exception sequences of ARM Cortex-M3?	[8M]
	b)	Define the term "Interrupt Latency"?	[2M]
6.		Demonstrate the architecture of LPC 17xx family of microcontroller with a neat block diagram.	[10M]
		OR	
7.		Describe each register used to configure the PWM module in the LPC17xx family of microcontrollers.	[10M]

8. a) Explain briefly what Multi port memory is and how it works in Programmable DSP Processors. [6M]
   b) Describe the features of the TI DSP family of Processors. [4M]

OR

9. Explain the architecture of the TI DSP processor with a block diagram. [10M]

10. Draw a neat diagram to illustrate the architecture of the DSP TMS320C6000 processor. [10M]

OR

11. a) Outline the addressing modes of the DSP TMS320C6000 Processor. [5M]
    b) Summarize the DSP TMS320C6000 processor's Assembly Language Instructions. [5M]

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