Code No.: EC57203PE | R20 | H.T.No. | | | 8 | R | | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Regular) - September- 2022
SOC Design
(VLSI System Design)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: *1. Answer any FIVE questions. Each question carries 14 marks.*
2. All questions carry equal marks.
3. Illustrate your answers with NEAT sketches wherever necessary.

5X14=70

1.	a)	Explain the Design Strategies of ASIC.	[7M]
	b)	Differentiate CISC, RISC and NISC.	[7M]
2.	a)	Illustrate the Design Flow of NISC and its importance.	[7M]
	b)	Write a brief notes on the NISC and also its Advantages and Applications.	[7M]
3.	a)	Explain the Reconfigurable Techniques used in Customization of SoC.	[7M]
	b)	Write short notes on Static Timing Analysis and Clock Tree Design Issues and explain it with diagrams.	[7M]
4.	a)	What are the different Voltage Scaling Techniques used for Low Power SoC Design.	[7M]
	b)	What are the various building blocks used for SoC Design and explain their Optimization Method.	[7M]
5.	a)	Explain the two different Technology Approaches for the Process of Synthesis.	[7M]
	b)	Illustrate the various HDL coding Techniques used for the Minimization of Power Consumption.	[7M]
6.	a)	Explain the Architectural issues and its impact on the SoC design.	[7M]
	b)	What is an ASIC? And explain the design approach of SoC framework.	[7M]
7.	a)	Explain the Design and Verification of ASIP.	[7M]
	b)	Explain the significance of Generic Netlist Representation for Processors with an example.	[7M]
8.	a)	Explain the Low Power FPGA.	[7M]
	b)	Compare Gate Level, Switch Level and Transistor Level Simulation Techniques.	[7M]

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