Code No.: R22EC~~57203PE32~~ 57232PE

R22	H.T.No.			8	R					

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Regular) – September- 2023
SOC DESIGN
(VLSI SD)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1. a)	Differentiate Between RISC and NISC.	[1M]
b)	What is the advantage of ASIP over single purpose processor?	[1M]
c)	Mention the applications of NISC.	[1M]
d)	Write any two advantages of NISC.	[1M]
e)	What is the purpose of design verification?	[1M]
f)	What is simulation in design?	[1M]
g)	Write about significance of clock gating.	[1M]
h)	What is meant by Dynamic clock frequency scaling?	[1M]
i)	What is the role of Graph theory?	[1M]
j)	What is meant by Dark silicon?	[1M]

PART-B **(50 Marks)**

2.	Explain about ASIC design methodologies	[10M]
	OR	
3.	Explain the Layouts of CISC, RISC and NISC.	[10M]
4.	Explain about NISC control word methodologies.	[10M]
	OR	
5.	Explain the block diagram of GNR schema for NISC architecture.	[10M]
6.	Explain any four types of simulations.	[10M]
	OR	
7.	What is meant by clock tree design and explain various design issues.	[10M]
8.a)	How can AVS and DCFS be used to optimize in-chip conditions?	[6M]
b)	Mention the applications of AVS & DCFS.	[4M]
	OR	
9.	Mention various power down techniques. Explain any two techniques.	[10M]
10.	Explain in detailed about synthesis report analysis for single core and multicore systems.	[10M]
	OR	
11.	Explain any three aspects of fault tolerance techniques.	[10M]

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