Code No.: EC57203PE | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Regular) – September - 2021
SOC Design
(VLSI System Design)

[Time: 3 Hours] **[Max. Marks: 70]**

1. *Answer Any **FIVE** Questions. Each Question Carries 14 Marks*
2. *All Questions Carry Equal Marks*
3. *Illustrate your answers with NEAT sketches wherever necessary.*

5X14=70

1.	a)	Classify the ASIC types? Explain them?	[7M]
	b)	Compare CISC, RISC and NISC approaches for SOC architectural issues?	[7M]
2.	a)	Explain the NISC Control Words methodology and their Applications and Advantages	[7M]
	b)	Explain Architecture Description Languages (ADL) for design and verification of Application Specific Instruction- set Processors.	[7M]
3.	a)	Explain the Low power FPGA Reconfigurable systems	[7M]
	b)	Analyze SoC related modelling of data path design and control logic	[7M]
4.	a)	Explain Architecture of Adaptive voltage scaling.	[7M]
	b)	Explain about Dynamic clock frequency and voltage scaling (DCFS)with neat sketch	[7M]
5.	a)	Distinguish between Technology independent and technology dependent approaches for synthesis.	[7M]
	b)	Explain with examples HDL coding techniques for minimization of power consumption.	[7M]
6.	a)	Explain the SoC design methodologies.	[7M]
	b)	Explain Application Specific Instruction Processor concepts.	[7M]
7.	a)	Explain about compilation and synthesis of embedded processors with necessity diagrams.	[7M]
	b)	Draw the modeling NISC Architecture and explain in briefly?	[7M]
8.	a)	Differentiate Different simulation modes with suitable examples.	[7M]
	b)	Explain about clock tree design issues.	[7M]

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