6/2/24

Code No.: IT301ES | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Supply) - February- 2024
ANALOG & DIGITAL ELECTRONICS
(Common to IT, CSM & AI&DS)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a)	Discuss about diode switching times.	[2M]
b)	What is regulation? Define its percentage of regulation.	[2M]
c)	Define current amplification factor.	[2M]
d)	Illustrate CE cutoff region and saturation region.	[2M]
e)	Compare BJT and FET.	[2M]
f)	Define de Morgan laws.	[2M]
g)	What is an essential prime implicant?	[2M]
h)	Define Magnitude Comparator.	[2M]
i)	Compare combinational and sequential circuits.	[2M]
j)	What is state diagram?	[2M]

PART-B **(50 Marks)**

2.	Explain the operation of P-N Junction Diode with its V-I Characteristics.	[10M]
	OR	
3.	Draw the circuit diagram and waveforms of Bridge full wave rectifier and explain its working with necessary equations.	[10M]
4.	Explain CE configuration with the help of input and output characteristics.	[10M]
	OR	
5.	How transistor acts as a switch. Explain with different switching times.	[10M]
6.	Explain the operation of Depletion mode MOSFET with its symbol and characteristics.	[10M]
	OR	
7. a)	Realize XOR gate using universal gates.	[5M]
b)	Explain the operation of TTL with neat diagram.	[5M]
8. a)	Minimise the following Boolean function using K-map. $F=\Sigma m(0,3,4,7,8,10,12,14)+d(2,6)$	[5M]
b)	Construct a 3*8 decoder using logic gates and its truth table.	[5M]
	OR	
9. a)	Design the 4-bit binary Adder-Subtractor with suitable diagram.	[5M]
b)	Design a 4- input priority encoder	[5M]
10.	Draw and explain SR flip flop with truth table and find characteristic equation	[10M]
	OR	
11.	Draw and explain the logic diagram of 4-bit ring counter with the help of timing diagrams.	[10M]

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