CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Regular) - February- 2024
ANALOG & DIGITAL ELECTRONICS
(Common for IT, CSM)

[Time: 3 Hours]   [Max. Marks: 60]

Note: This question paper contains two parts A and B.
         Part A is compulsory which carries 10 marks. Answer all questions in Part A.
         Part B consists of 5 Units. Answer any one full question from each unit. Each question
         carries 10 marks and may have a, b, c as sub questions.

PART-A   (10 Marks)

1. a) Draw the piecewise linear volt-ampere characteristic of a p-n diode. [1M]
   b) Define peak inverse voltage. [1M]
   c) What are transistor regions? [1M]
   d) What are the classifications of Multistage amplifiers? [1M]
   e) Draw the symbol of universal gates. [1M]
   f) Draw the CMOS inverter circuit. [1M]
   g) Define Multiplexer. [1M]
   h) Draw 1-bit digital comparator. [1M]
   i) Define a sequential system and how does it differ from a combinational system? [1M]
   j) Define a ROM. [1M]

PART-B   (50 Marks)

2. a) Explain V-I characteristics of a PN junction diode. [5M]
   b) Determine the forward bias voltage applied to silicon diode to cause a forward current [5M] of 10mA and reverse saturation current $I_o = 25 \times 10^{-7}$ A at room temperature

OR

3. Explain the action of a full-wave rectifier and give waveforms of input and output [10M] voltages.

4. What is an amplifier? And explain various types of amplifiers. [10M]

OR

5. A CE amplifier is driven by a voltage source of internal resistance $R_S = 800$ Ω, and [10M] the load impedance is a resistance $R_L = 1000$ Ω. The h-parameters are $h_{ie} = 1$ k Ω, $h_{re} = 2 \times 10^{-4}$, $h_{fe} = 50$ and $h_{oe} = 25$ μA/V. Compute the current gain A_I, input resistance R_i, voltage gain A_V and output resistance R_O using exact analysis and using approximate analysis.

6. Draw the small signal equivalent circuit of FET amplifier in CS connection and derive [10M] the equations for voltage gain, input impedance and output impedance.

OR

7. a) Explain the De Morgan's Laws. [5M]
   b) Simplify the following Boolean expressions [5M]
       i. A+AB+ABC+ABCD   ii. AB+BC+A'C

8. Implement full adder with two half adders and an OR gate. [10M]

OR

9. Minimize the following Boolean functions using K-map and draw the logic diagram [10M] using NAND gates.
    F (A,B,C,D) = Σm (1,3,5,8,9,11,15) +d (2,13)

10. Convert the S R Flip Flop to T flip Flop. [10M]

OR

11. Explain how a shift register is used as a converter from i) serial-to-parallel data and [10M] ii) parallel-to-serial data.

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