Code No.: R22CS302PC

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## CMR ENGINEERING COLLEGE: : HYDERABAD UGC AUTONOMOUS

II-B.TECH-I-Semester End Examinations (Regular) - February- 2024 COMPUTER ORGANIZATION AND ARCHITECTURE (Common for CSE, IT, CSC, CSD, CSM)

[Time: 3 Hours] [Max. Marks: 60] Note: This question paper contains two parts A and B. Part A is compulsory which carries 10 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions. PART-A (10 Marks) What is Bus? Draw the single bus structure. 1. a) [1M] What is an instruction cycle? b) [1M] What is Accumulator register? c) [1M] d) What are the advantages of microprogrammed control unit? [1M] Write equal signed-magnitude of the +14. [1M]How the floating-point numbers are represented and used in digital arithmetic [1M] operations? Define Asynchronous data transfer. [1M] h) What is Interrupt? [1M] i) Define parallel processing. [1M] What is inter process communication. [1M] PART-B (50 Marks) Draw the flowchart for instruction cycle and explain. 2. [10M] OR 3.a) Compare and Contrast the Computer Design and Computer Architecture. [5 M] Compare hardwired control with microprogrammed control. [5 M] Explain the design of control unit. 4. [10M] OR 5. What is a micro program? Explain the flowchart of a micro program for the Add src, [10M] Rdst instruction which adds the source operand to the contents of the register Rdst and places the sum in Rdst. Explain the floating point addition- subtraction unit with a neat diagram. 6. [10M] With the help of hardware schematic and flowchart, explain the implementation of 7. [10M] Multiplication operation in computers. What is an auxiliary memory? Explain. 8.a) [5 M] What is a cache memory? What are cache hit and cache miss? Define hit ratio. [5 M] Discuss about Main Memory and its types in details. 9. [10M] 10. Illustrate about RISC pipeline vector processing. [10M]

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What are multi processors? Discuss their characteristics.

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