Code No.: EC744PE | R20 | H.T.No. | | | 8 | R | | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
IV–B.TECH–I–Semester End Examinations (Supply) - April- 2024
DIGITAL CMOS IC DESIGN
(ECE)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a) Draw the circuit diagram of a Pseudo NMOS inverter. [2M]
   b) Define Fall time. [2M]
   c) Write the expressions for Sum and Carry in a Half-Adder circuit. [2M]
   d) Write any three advantages of CMOS technology. [2M]
   e) Write the truth table of a Two input NOR gate. [2M]
   f) Draw the circuit schematic of Two-inverter basic bistable element. [2M]
   g) What is a Transmission gate? [2M]
   h) Write about Charge leakage in MOS transistors. [2M]
   i) What is the purpose of a Row address decoder? [2M]
   j) Compare PROM, EPROM and EEPROM. [2M]

PART-B **(50 Marks)**

2. Illustrate transistor equivalency with circuit diagram and drain current expressions. [10M]

OR

3. Draw the circuit diagram of a typical CMOS inverter. Explain its operation and derive the expression for voltage gain. [10M]

4. Design a one-bit full-adder circuit using CMOS transistor schematic. [10M]

OR

5. Draw the Two-input NMOS depletion-load NAND gate. Explain its operation in each with its truth table. [10M]

6. Discuss the operation of a CMOS negative (falling) edge-triggered master-slave D flip-flop along with its circuit diagram. [10M]

OR

7. Illustrate the operation of a CMOS SR latch circuit based on NAND2 gates along with its truth table. [10M]

8. Draw the circuit diagram of a Three stage depletion-load nMOS dynamic shift register circuit driven with Two-phase clocking scheme. Explain its operation. [10M]

OR

9. Draw the logic diagram of Domino CMOS logic gate and Cascaded domino CMOS logic gates. Also explain its working principle. [10M]

10. Explain about the working principle of Full CMOS static RAM cell. [10M]

OR

11. Draw the diagram of a typical Random-Access Memory array organization and explain its various inner circuit blocks. [10M]

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