Code No.: R22EC305ES | R22 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Regular) - February- 2024
DIGITAL LOGIC DESIGN
(CSD)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1. a) The numbers $(432.2)_8$ and $(1101.01)_2$ in base converts into base 10. [1M]
   b) Explain the EXCLUSIVE-OR operation. [1M]
   c) Draw a logic diagram of EXOR gate using NOR gates. [1M]
   d) Obtain the PI, EPI for given function $f(x, y,z) = \sum m(0, 2, 3, 5)$. [1M]
   e) Compare between combination circuit and sequential circuits. [1M]
   f) How many 4X1 MUX required to implementation of 32 X1 MUX? [1M]
   g) Explain the D flip flop Truth table. [1M]
   h) How many used and unused states for decade counter? [1M]
   i) Define Programmable Array Logic (PAL) and its role in digital circuits? [1M]
   j) Explain the memory decoding. [1M]

PART-B **(50 Marks)**

2. Convert the following numbers in the way specified: [10M]
   i. $(11001010.0101)_2$ to base 10
   ii. $(53.1575)_{10}$ to base 2
   iii. $(11001101.0101)_2$ to base 16
   iv. $(315)_8$ to base 10
   v. $(1001010101)_2$ to Gray code

OR

3. i. Determine the canonical sum-of-products representation of the functions $f(x, y, z) = x + (x'y' + x'z)$ [10M]
   ii. To simplify the expression $T(x, y, z) = (x + y)[x'(y' + z')] + x'y' + x'z'$

4. Minimize the switching functions $f(w, x, y, z) = \sum m(1, 3, 4, 5, 9, 10, 11) + \sum_d(6, 8)$ [10M]

OR

5. Determine the minimal sum-of-products expression for $f(w, x, y, z) = \sum m(0, 2, 8, 10, 12, 14) + \sum_d(3, 5)$ and draw a NOR GATE circuit diagram. [10M]

6. Implementation of full subtractor using 3 to 8 Decoder. [10M]

OR

7. Design the 2- bit magnitude comparator. [10M]

8. What are the disadvantages of JK Flip Flop? Draw a JK flip flop logic diagram and characteristic equation. [10M]

OR

9. Design a 4 bit ring counter. [10M]

10. Discuss how PALs are used in combinational and sequential logic and List the advantages of using a PLA in comparison to fixed logic circuits. [10M]

OR

11. Explain the Random-Access Memory and discuss with details. [10M]

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