Code No.: EC302PC

R20   H.T.No. [ ][ ][8][R][ ][ ][ ][ ]

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Supply) - February- 2024
DIGITAL SYSTEM DESIGN
(ECE)

[Time: 3 Hours]   [Max. Marks: 70]

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 20 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A   (20 Marks)

1. a) Given that $(292)10 = (1204)b$ determine the value of b.   [2M]
   b) State De Morgan's theorem and Duality.   [2M]
   c) Define Minterm and Maxterm.   [2M]
   d) Write the truth table of priority encoder.   [2M]
   e) Write the difference between Latch and Flip flop.   [2M]
   f) What is shift register? Give the classification of them?   [2M]
   g) How many memory locations are addressed using 18 address bits?   [2M]
   h) What is the size of the decoder in 32x10 ROM?   [2M]
   i) Draw the DTL OR gate.   [2M]
   j) Draw the symbol of NMOS and PMOS transistor.   [2M]

PART-B   (50 Marks)

2. Convert the following binary numbers to both 1's and 2's complement (i) 101 [10M]
   (ii) 1011.01 (iii) 11.101 (iv) 10111.10 (v) 0.101.

                                    OR

3. Realize X-OR gate operation using (i) only NAND gates (ii) only NOR gates.   [10M]

4. Obtain (i) Sum of products form and (ii) Product of sums form for   [10M]
   F=x'z'+y'z'+yz'+xy.

                                    OR

5. With a neat design procedure, explain the implementation of a 2-bit Magnitude   [10M]
   Comparator.

6. Give the characteristic table, Truth table, characteristic equation and excitation table   [10M]
   for T and DFF.

                                    OR

7. Draw and explain 4-bit Universal shift register.   [10M]

8. Describe the design procedure of synchronous finite state machine (FSM) by taking   [10M]
   serial binary adder as example.

                                    OR

9. Give the comparison between PROM, PLA and PAL.   [10M]

10. Compare TTL, ECL and CMOS.   [10M]

                                    OR

11. What is meant by Tristate logic? Draw the circuit of Tristate TTL logic and explain   [10M]
    the functions.

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