Code No.: EC622PE | R20 | H.T.No. | | | 8 | R | | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
III–B.TECH–II–Semester End Examinations (Regular) - June- 2024
FPGA PROGRAMMING
(ECE)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A

(20 Marks)

1. a) What is a Programmable Read Only Memory (PROM)? [2M]
   b) Identify Configurable Logic Blocks (CLBs) in FPGA architectures? [2M]
   c) What does UDM-PD stand for? [2M]
   d) Name two common Hardware Descriptive Languages. [2M]
   e) How are signals declared in a Dataflow description? [2M]
   f) Define Behavioral Description in the context of HDLs. [2M]
   g) How are state machines represented in Structural Descriptions? [2M]
   h) Define Switch-Level Description and its significance in HDLs. [2M]
   i) Describe Tasks in Verilog and their usage. [2M]
   j) What are Assertion Languages used for in verification? [2M]

PART-B

(50 Marks)

2. Demonstrate the architecture of CPLDs. Highlight the roles of Function Blocks, I/O Blocks, Clock Drivers, and Interconnects in CPLD functionality. [10M]

OR

3. Compare SRAM and Anti-fuse programming technologies in FPGAs. [10M]

4. Develop different verification stages of the Universal Design Methodology. [10M]

OR

5. Compare and contrast the structures of VHDL and Verilog modules. Highlight their similarities and differences with examples. [10M]

6. Explain the structure of a Dataflow description in HDLs. Include examples of signal declaration and assignment statements. [10M]

OR

7. Write VHDL code in behavioural description of a D-latch using signal assignment statements and if statements. [10M]

8. Explain the concept of binding and its importance in Structural Descriptions. [10M]

OR

9. Model a switch level description of 4:1 Multiplexer with active high enable. [10M]

10. Criticize the concept of Procedures in VHDL. Provide examples to illustrate their usage and advantages in HDL design. [10M]

OR

11. Examine the concept of formal verification in HDL design. How does formal verification differ from simulation-based verification? [10M]

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