Code No.: EC622PE | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
III–B.TECH–II–Semester End Examinations ((Supply) - January- 2024
FPGA PROGRAMMING
(ECE)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each questioncarries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a)	Explain the difference between PLA and PAL	[2M]
b)	Explain the difference between CPLD and FPGA	[2M]
c)	What is the difference between Scalars and Vectors in Verilog module.	[2M]
d)	Define with example, the following terms related to VHDL. i. Entity ii. Architecture	[2M]
e)	Define Behavioral model.	[2M]
f)	List the operators in VHDL.	[2M]
g)	Define keywords in Verilog HDL.	[2M]
h)	Explain Process statement in VHDL with example.	[2M]
i)	Distinguish betweenVHDL and Verilog HDL.	[2M]
j)	Define simulation.	[2M]

PART-B **(50 Marks)**

2.	Design a combinational logic circuit using PLA and PAL.	[10M]
	OR	
3.	Explain the Architecture of FPGA with its advantages and applications.	[10M]
4.a)	Explain the TOP down design methodology relevant to hardware modeling usingVerilog HDL.	[5M]
b)	Discuss various descriptive styles available for hardware modeling usingVerilog HDL.	[5M]
	OR	
5.	Explain the procedure for design of state machine using one hot encoding.	[10M]
6.	What are the data types available in Verilog HDL? Discuss them with necessary syntax with an example.	[10M]
	OR	
7.	Explain in detail different modeling styles of VHDL with suitable examples.	[10M]
8.	Explain combinational and sequential behavior of user defined primitives in Verilog HDL.	[10M]
	OR	
9.	Develop Verilog code for NMOS Two input NOR Gate in switch level model.	[10M]
10.	Explain in detail different simulation types with an example.	[10M]
	OR	
11.	What are the design verification tools available? Explain any one of them.	[10M]

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