Code No.: R22EC57102PC

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## CMR ENGINEERING COLLEGE: : HYDERABAD UGC AUTONOMOUS

## I–M.TECH–I–Semester End Examinations (Regular) - March- 2024 MICROCONTROLLERS & PROGRAMMABLE DIGITAL SIGNAL PROCESSORS (VLSISD)

[Time: 3 Hours]

[Max. Marks: 60]

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 10 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

	PART-A (1	10 Marks)	
. a)	List out the applications of Cortex-M3 processor.		[1M]
b)	What is program counter?		[1M]
c)	Give system exceptions.		[1M]
d)	Draw the exception vector table.		[1M]
e)	What is the importance of WDT?		[1M]
f)	How many timers are there in LPC 17xx microcontroller?		[1M]
g)	Recall about multi-port memory.		[1M]
h)	List the applications of PDSP.		[1M]
i)	Write a short note on TMS320C6000.		[1M]
j)	Define cross path.		[1M]
	PART-B	(50 Marks)	
2.	Draw and explain the block diagram of ARM Cortex-M3 processor.		[10M]
2.	OR		F103 f7
3.	Analyse the operation of three-Stage Pipeline in the ARM Cortex-M3 processor.		[10M]
	CANCELLOV TO		[5M]
4.	(a) Illustrate about SYSTICK Timer.		[5M]
	(b) Give in detail explanation on Interrupt Latency.		
	OR	of timing	[10M]
5.	Explain the Interrupt inputs and pending behaviour in Cortex M3 processor with the help	01 11111111	
	waveforms.		
6	Describe the features and functionalities of LPC 17XX general purpose I/O (GPIO).		[10M]
6.	OR		
7.	Discuss the following interfaces		[10M]
/.	(a) RTC (b) WDT		
	(a) KTC		
8.	Explain the architectural structure of P-DSP-MAC Unit.		[10M]
0.	OR		54.03.57
9.	With neat diagram explain the Harvard architecture for programmable DSP Processors.		[10M]
			[10M]
10.	Explain the block diagram of Very Long Instruction Word (VLIW) architecture.		[10M]
	OR		[10M]
11.	With suitable examples explain the assembly instructions for arithmetic operations.		LIONI
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