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CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Regular) – August- 2024
SOC DESIGN
(VLSI SD)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions

PART-A **(10 Marks)**

1.	a)	Define ASCII and its role in computer systems.	[1M]
	b)	Which architecture typically has better pipeline efficiency, RISC or CISC?	[1M]
	c)	How does NISC improve efficiency and performance?	[1M]
	d)	Why is hardware customization significant in NISC?	[1M]
	e)	What is the primary purpose of functional simulation?	[1M]
	f)	Mention the strategies used to minimize interconnect impact and address clock tree design issues.	[1M]
	g)	How does dynamic clock frequency and voltage scaling (DCFS) improve power efficiency?	[1M]
	h)	Why is power consumption verification crucial in low power SoC design?	[1M]
	i)	Compare Single core and Multi core systems.	[1M]
	j)	Define concept of graph theory.	[1M]

PART-B **(50 Marks)**

2.	Compare the complexity of instruction sets in RISC and CISC architectures, highlighting the differences in the number of instructions, addressing modes, and instruction formats.	[10M]
	OR	
3.	Explain the concept of Application Specific Instruction Processors (ASIPs) and their advantages over general-purpose processors.	[10M]
4.	Discuss the flexibility offered by NISC in hardware customization.	[10M]
	OR	
5.	Describe about the emerging trends in ASIP design, such as machine learning integration, advanced fabrication technologies, and reconfigurable architectures.	[10M]
6.	Explain how verification vectors are used in different simulation modes to ensure the correctness and reliability of the design.	[10M]
	OR	
7.	Explain how these factors influence the design of data path and control logic.	[10M]
8.	Describe the various low power system techniques used in SoC design, including power gating, clock gating, and adaptive voltage scaling (AVS).	[10M]
	OR	
9.	Analyze the importance of power consumption verification in low power SoC design. What methods are used to verify power consumption, and why is this step crucial?	[10M]

10. Describe the importance of graph connectivity and components in ensuring the reliability and efficiency of synthesized designs. [10M]

OR

11. Explain the key principles and methodologies used to achieve fault tolerance, such as redundancy, error detection and correction and fail-safe mechanisms. [10M]

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