Code No.: EC603PC | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
III–B.TECH–II–Semester End Examinations (Regular) - June- 2024
VLSI DESIGN
(ECE)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a)	Define the Moore's law.	[2M]
b)	Define MOS transistors threshold voltage.	[2M]
c)	Explain about CMOS inverter.	[2M]
d)	Examine the scaling factors of MOS circuit.	[2M]
e)	Write a short note on wiring capacitance.	[2M]
f)	Define fan-in and fan out.	[2M]
g)	Difference between SRAM and DRAM.	[2M]
h)	Write a short note on zero/one detectors.	[2M]
i)	Difference between PLA and PAL.	[2M]
j)	What is the need of testing?	[2M]

PART-B **(50 Marks)**

2.	Write the fabrication steps of NMOS transistor with neat diagrams.	[10M]
	OR	
3.	List the advantages and disadvantages of CMOS technology over Bipolar technology.	[10M]
4.	Derive the equation for pull-up to pull down ratio (Z_{pu}/Z_{pd}).	[10M]
	OR	
5.	Explain the steps involved in VLSI design flow.	[10M]
6.	Discuss about the any two alternative gate circuits.	[10M]
	OR	
7.	What is switch logic give example?	[10M]
8.	Explain Barrel shifter with a neat diagram.	[10M]
	OR	
9.	Design and implement 4-bit ripple carry adder.	[10M]
10.	Explain about PLA and PAL with neat schematic diagram.	[10M]
	OR	
11.	Compare simple PLDs, CPLDs and FPGAs.	[10M]

****