Code No.: EC603PC | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
III–B.TECH–II–Semester End Examinations (Supply) - January- 2024
VLSI DESIGN
(ECE)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a)	Define g_m of MOS Transistor.	[2M]
b)	What is pull down device?	[2M]
c)	Draw the Stick Diagram for Two inputs NOR Gate.	[2M]
d)	Compare Stick and Layout Diagrams.	[2M]
e)	Define Fan-in and Fan-out.	[2M]
f)	What is CMOS Domino Logic?	[2M]
g)	Compare SRAM and DRAM.	[2M]
h)	What is Booth's algorithm?	[2M]
i)	Explain the principle of Built-in-Self test.	[2M]
j)	How CPLD is different from FPGA?	[2M]

PART-B **(50 Marks)**

2.	What are different pull ups? Explain their working with neat circuit diagram and also compare them.	[10M]
	OR	
3.	Derive the Pull-up to Pull-down ratio(Zpu/Zpd) for Inverter driving Pass Transistors.	[10M]
4.	Discuss with an example Lambda (λ) based transistor Design Rules.	[10M]
	OR	
5. a)	Draw the static CMOS logic circuit for the following expressions i) Y= (ABCD)′ ii) Y= [D(A+BC)]′	[6M]
b)	Draw the Layout Diagram for CMOS Inverter.	[4M]
6. a)	Describe the methods for driving large capacitive loads.	[5M]
b)	Design a 2-input Multiplexer using CMOS transmission gates.	[5M]
	OR	
7.	Describe about the choice of fan – in and fan – out selection in gate level design.	[10M]
8.	Design and implement 4-bit Ripple Carry Adder.	[10M]
	OR	
9.	Compare various Memories in detail with their architectures.	[10M]
10. a)	Explain chip level test techniques.	[5M]
b)	What is CPLD? Draw its basic structure and give its applications.	[5M]
	OR	
11.	Explain the architecture of FPGA. What are the advantages of FPGA?	[10M]

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