Code No.: R22EC301ES | R22 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Regular) - December- 2024
ANALOG & DIGITAL ELECTRONICS
(Common for IT, CSM)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1. a)	Draw half wave rectifier circuit diagram.	[1M]
b)	Draw a PN Junction diode characteristic with effect of temperature.	[1M]
c)	Compare CE, CB, CC configuration.	[1M]
d)	Draw self-bias circuit diagram.	[1M]
e)	Draw the MOSFET symbols.	[1M]
f)	List the universal logic gates.	[1M]
g)	Define Minterms and Maxterms of Boolean expressions.	[1M]
h)	Realize the EXOR logic gate using NAND gates.	[1M]
i)	Define the flip-flop and list the type of flip-flops.	[1M]
j)	Compare synchronous and asynchronous counters.	[1M]

PART-B **(50 Marks)**

2.	Explain the full wave rectifier with capacitor filter.	[10M]
	OR	
3.	Explain the Diode switching times and diode resistance.	[10M]
4.	Explain input and output characteristics of transistor in CB configuration with neat diagram.	[10M]
	OR	
5.	Explain about RC coupled amplifier.	[10M]
6.	Explain the low frequency CS amplifier.	[10M]
	OR	
7.	Discuss the NOR DTL and TTL logic families.	[10M]
8.	Reduce the Boolean expression using k map $F(A,B,C,D)=\sum m(1,3,5,9,11)+d(2,4,13)$	[10M]
	OR	
9.	Reduce the Boolean expression using k map $F(A,B,C,D)=\sum m(1,3,4,9,13)+d(2,5,12)$	[10M]
10.	Design of 3 bit up counter using asynchronous counter.	[10M]
	OR	
11.	Explain the JK Flip Flop with characteristic table.	[10M]

****