

Code No.: EC744PE

R20

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CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
IV-B.TECH-I-Semester End Examinations (Regular) - November- 2024
DIGITAL CMOS IC DESIGN
(ECE)

[Time: 3 Hours]

[Max. Marks: 70]

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A

(20 Marks)

1. a) Define Rise Time and Fall Time. [2M]
- b) Draw the Pseudo NMOS realization of exclusive OR function. [2M]
- c) Draw the symbol of CMOS transmission gate. [2M]
- d) What are the advantages of CMOS logic? [2M]
- e) What are the characteristics of SR Latch? [2M]
- f) Draw the D Latch using CMOS Logic. [2M]
- g) Draw the synchronous dynamic Pass Transistor Circuit. [2M]
- h) Write the definition of Voltage Bootstrapping. [2M]
- i) Define a single bit Dynamic RAM cell. [2M]
- j) Explain the Principle of SRAM. [2M]

PART-B

(50 Marks)

2. Perform the Rise time and Fall time analysis of Pseudo NMOS Inverter logic with one example. [10M]
- OR**
3. Define Threshold Voltage of CMOS Inverter. Express threshold voltage and discuss the dependency of V_T on various parameters. [10M]
 4. Design and implement AOI and OIA logics using CMOS. [10M]
- OR**
5. Realize the following Boolean expression $Y = (AB + BC + CA)'$ by using CMOS logic. [10M]
 6. Write short notes on SR latch in sequential MOS logic. [10M]
- OR**
7. Explain Clocked SR Flip Flop operation using appropriate circuit diagram. [10M]
 - 8.a. Write a short note on any one of the High performance Dynamic CMOS circuits. [4M]
 - b. Explain about Synchronous dynamic pass transistor circuit with an example. [6M]
- OR**
9. Realize CMOS Dynamic Latch using transmission gate and explain the Set and Reset conditions of the Latch. [10M]

- 10.a. Write about the leakage currents in SRAM. [5M]
- b. Draw the circuits of SRAM and DRAM. [5M]

OR

11. Draw the DRAM cell and explain its Read and Write operation and compare DRAM cell with SRAM cell. [10M]
